MODEL ACCURACY FOR A SMART POWER ASIC CHIP SET FOR SPACE

J. Ricart, D. González, R. Cabás, F. Gutiérrez (ARQUIMEA INGENIERÍA SLU).
M. García (UC3M)
D. Peña, L de la Fuente (EADS-CASA-Espacio)

This presentation and its contents are considered as ARQUIMEA’s proprietary and as such they cannot be fully or partially distributed to third parties without the written authorization of ARQUIMEA INGENIERÍA S.L.
OBJETIVES OF THE PRESENTATION

- Present the iteration process followed when a radiation issue was found and how it was overcome

- Present a comparison between the simulation models and the electrical tests performed on the final ASIC for two foundry runs with different process parameters.

- Give an overview of the design and qualification flow of an Analog ASIC for space use and the supply chain
REDSAT PROJECT BACKGROUND

- ASIC Chip set originally conceived as a single mixed signal ASIC to perform control, power and monitoring of the RF chain of the DRA-ELSA Antenna based on On Semi’s I3T80 technology \(^{(1)}\).

- Due to the complexity/timing requirements of developing a RH Digital Library for the chosen technology \(^{(2)}\), the design was split into one analog and mounted in a hybrid as bare dies.

\(^{(1)}\) None of the technologies with RH Digital libraries allowed the implementation of the power MOSFETS located in the Analog design.

\(^{(2)}\) ARQUIESEA is currently developing a RH Digital Library for this technology
The digital ASIC has a dual functionality: Controller or Actuator (shift register).

Implemented using the DARE library

Already validated for space use: TID 120Krad (parametric), SEU and Latch up Free. 😊
The analog ASIC offers smart power capabilities and current and temperature measurements.

Implemented on the I3T80 technology from ON Semiconductor using radiation hardening by design techniques.

Meets radiation requirements: 50Krad TID (parametric), SEL free (> 67.5 MeV cm²/mg).

The qualification campaign is ongoing pending on Life test results.
RADIATION NON CONFORMANCE

- After radiation hardening by design techniques were used in the design\(^{(1)}\) it was not expected to find any major issues with the radiation test.

- However...Things happen.

\(^{(1)}\) See ARQUIMEA’s high power distribution, control and monitoring ASIC(smart power) presentation on AMICSA 2010 proceedings.
RADIATION NON CONFORMANCE

- SEL tests showed a LET threshold of 22.5 MeV cm mg² cm⁻¹ 😞

- The latch-up was not destructive since the current was limited to 400mA.

- 400 to 500 s range
- SEL enlarged
- Sustaining time is 10s
- Off time is 0.5s
RADIATION NON CONFORMANCE (ANALYSIS)

➢ An analysis on the radiation hardening techniques to avoid SEL in the core design was held and no issue was identified.

➢ Attention was then paid on the digital I/O pads which had not been modified for Latch Up immunity.

➢ The Digital I/O pads had an enable circuitry where the PMOS and NMOS transistors were not isolated.
Laser tests confirmed the hypothesis: The LU sensitive areas were located in the digital I/O Pads, the rest of the core was LU free.

LU sensitive structures detected during laser scan on Input (a) and Output (b) pads.
RADIATION NON CONFORMANCE (PAD MODIFICATION)

- The digital I/O PADS had to be modified to make them LU free

- Several options were evaluated and considered between ESA, ON-SEMI and ARQUIMEA

- The chosen solution only required a metal masks fix

- Fortunately some back-up lots were left at metal mask level at the foundry
ANALOG ASIC RUN 2

- Run 2 with the metal mask fix was fabricated from the back-up lot

- However...Things happen.
ANALOG ASIC RUN 2 (BODY FACTOR)

- It turned out that the body factor of the P channel 10x10 was too high in the back up lot. (the body factor is a process parameter out of the designer control).

- In order to validate the lot:
  1. Simulations were performed with a corner that reproduced the body factor drift.
  2. ESD test was performed at two wafers and one wafer was sawed and some dice was assembled to be electrically tested.

- At the same time some of the encapsulated dies were prepared for radiation test to see if the Latch up sensitivity improved or not.
ANALOG ASIC RUN 2 (SEL INMUNITY)

- Latch Up test showed that the RUN 2 of the ASIC was Latch up free at least up to 67.5 MeV cm$^2$/mg

[1] OBJECTIVES
[2] PROJECT BACKGROUND
[3] RADIATION NC
[4] ANALOG ASIC RUN 2
[5] SIMULATION VS VALIDATION
[6] SUPPLY CHAIN QUALIFICATION & LAT

AMICSA 2012
SIMULATION VS VALIDATION (ICC)

- Simulation $I_{CC}$ corner TYP
- Simulation $I_{CC}$ corner AWCS
- Measures EDS run 1
- Measures EDS run 2

Current value [A]

Simulation time [s]

Measured sample

$10^{-2}$
[1] OBJETIVES
[2] PROJECT BACKGROUND
[3] RADIATION NC
[4] ANALOG ASIC RUN 2
[5] SIMULATION VS VALIDATION
[6] SUPPLY CHAIN
QUALIFICATION & LAT

AMICS A 2012
SIMULATION VS VALIDATION (VREF2)

- Vref 2 measured on samples run 1
- Vref 2 measured on samples run 2

- Median EDS measures Vref 2 run 1
- Median EDS measures Vref 2 run 2
- Simulation Vref 2 Typical
- Simulation Vref 2 corner AWCS

Voltage [V] vs Time [s]

Sample measured

0.905
0.90
0.895
0.89
[1] OBJECTIVES
[2] PROJECT BACKGROUND
[3] RADIATION NC
[4] ANALOG ASIC RUN 2
[5] SIMULATION VS VALIDATION
[6] SUPPLY CHAIN QUALIFICATION & LAT

ASIC definition and requirements specification
- USER: EADS ASTRIUM CASA ESPACIO

QUALIFICATION ACTIVITIES
- SUPPLIER (ARQUIMEA)

TECHNOLOGY SELECTION, PRELIMINARY DESIGN DEVELOPMENT PLAN
- SUPPLIER: ARQUIMEA

DETAILS DESIGN AND VERIFICATION. PRELIMINARY ASIC SPECIFICATION
- SUPPLIER: ARQUIMEA

RUN1 MANUFACTURE
- FOUNDRIES
  ON SEMI (ANALOG ASIC)
  IMEC/UMC (DIGITAL ASIC)

QUALIFICATION ACTIVITIES
- SUPPLIER (ARQUIMEA)

FINAL ASIC SPECIFICATION
- SUPPLIER: ARQUIMEA

REDESIGN (IF APPLICABLE)
- SUPPLIER: ARQUIMEA

RUN 2 MANUFACTURE (IF APPLICABLE)
- FOUNDRIES
  ON SEMI (ANALOG ASIC)
  IMEC/UMC (DIGITAL ASIC)

LOT ACCEPTANCE TEST
- SUPPLIER: ARQUIMEA

DELIVERY OF PARTS
- SUPPLIER: ARQUIMEA

Approvals
- Responsible
LOT ACCEPTANCE FLOW OF ASIC DICE FOR HYBRID ASSEMBLY (ON RUN 2, IF APPLICABLE)

ON WAFER TEST
- TEST HOUSE: IMS FRAUNHOFER

DICE SELECTION AND CLASSIFICATION
- USER: ECE
- SUPPLIER: ARQUIMEA

WAFER SAWING/DICING
- TEST HOUSE: IMS FRAUNHOFER

LAT LOT ASSEMBLY (DICE RELATED TESTS)
- ASSEMBLY HOUSE: INDRA

PRECAP INSPECTION
- SUPPLIER: ARQUIMEA AND USER: ECE
- ASSEMBLY HOUSE: INDRA

ASSEMBLY CAPABILITY TEST 1 (BOND PULL & DIE SHEAR)
- ASSEMBLY HOUSE: INDRA

DICE FOR HYBRID QUALIFICATION*

DICE FOR FLIGHT* (HYBRID ASSEMBLY)

SCREENING (SEM, ESD, ELECT. CHARACTER., BURN-IN, SEAL TEST).
- TEST HOUSE: HIREX

RADIATION TEST (TID, SEE) - DELTA
- TEST HOUSE HIREX

RELIABILITY TEST (1000 H LIFE TEST)
- TEST HOUSE: HIREX

FAILURE ANALYSIS (IF APPLICABLE)
- TEST HOUSE (HIREX)

Approvals
- Responsible

* IN CASE OF SUCCESSFUL LAT OF RUN 2
Acknowledgements

EADS-CASA ESPACIO
ESA
ON SEMICONDUCTORS (Support)
UC3M (Digital ASIC design)
IMEC (Digital Backend and fabrication)
HIREX (Testing)
IMS FRAUNHOFER (On wafer Tests)
INDRA (Samples packaging)

And thank you for your attention!
Contact

Daniel González
Francisco Gutierrez

+34 627 49 54 10
dgonzalez@arquimea.com
fgutierrez@arquimea.com
http://www.arquimea.com