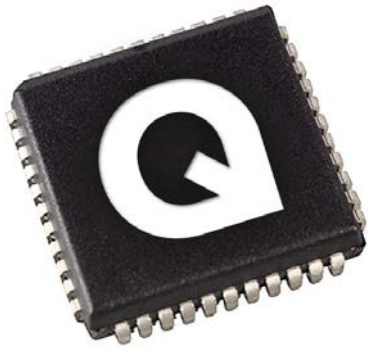

MODEL ACCURACY FOR A SMART POWER ASIC CHIP SET FOR SPACE

J. Ricart, D. González, R. Cabás, F. Gutiérrez (ARQUIMEA INGENIERíA SLU).

M. García (UC3M)

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OBJETIVES OF THE PRESENTATION

- Present the iteration process followed when a radiation issue was found and how it was overcome

- Present a comparison between the simulation models and the electrical tests performed on the final ASIC for two foundry runs with different process parameters.

- Give an overview of the design and qualification flow of an Analog ASIC for space use and the supply chain

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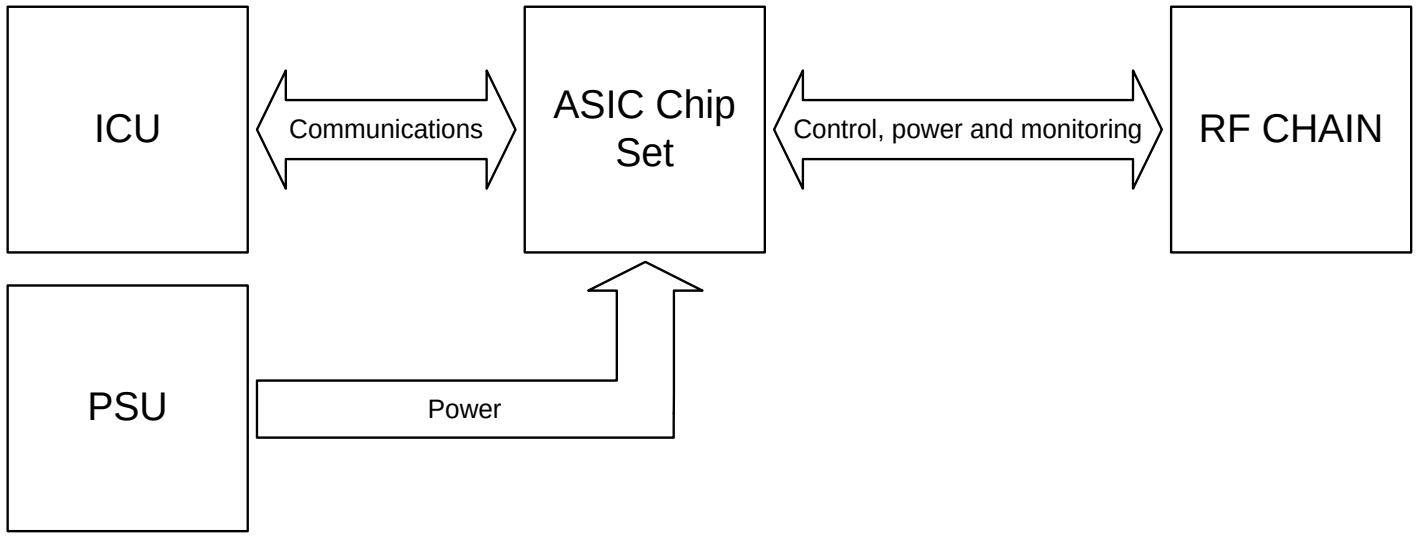
REDSAT PROJECT BACKGROUND

EADS CASA ESPACIO



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REDSAT PROJECT BACKGROUND

- ASIC Chip set originally conceived as a single mixed signal ASIC to perform control, power and monitoring of the RF chain of the DRA-ELSA Antenna based on On Semi's I3T80 technology (1).

- Due to the complexity/timing requirements of developing a RH Digital Library for the chosen technology (2), the design was split into one analog and mounted in a hybrid as bare dies.

(1) None of the technologies with RH Digital libraries allowed the implementation of the power MOSFETS located in the Analog design.
(2) ARQUIMEA is currently developing a RH Digital Library for this technology

REDSAT PROJECT BACKGROUND (DIGITAL ASIC)

- The digital ASIC has a dual functionality: Controller or Actuator (shift register).
- Implemented using the DARE library
- Already validated for space use: TID 120Krad (parametric), SEU and Latch up Free.

REDSAT PROJECT BACKGROUND (ANALOG ASIC)

- The analog ASIC offers smart power capabilities and current and temperature measurements.

- Implemented on the I3T80 technology from ON Semiconductor using radiation hardening by design techniques

- Meets radiation requirements : 50Krad TID (parametric), SEL free (> 67.5 MeV cm^2/mg) 

- The qualification campaign is on going pending on Life test results.

RADIATION NON CONFORMANCE

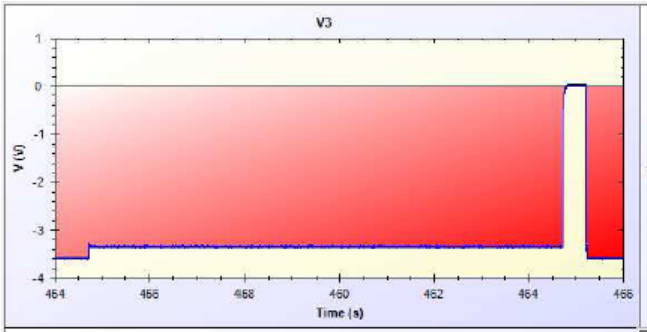
- After radiation hardening by design techniques were used in the design(1) it was not expected to find any major issues with the radiation test

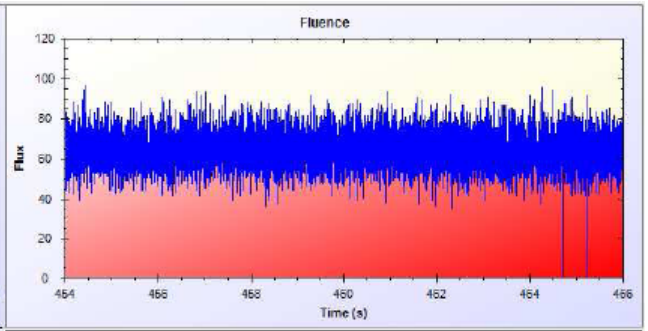
- However…Things happen.

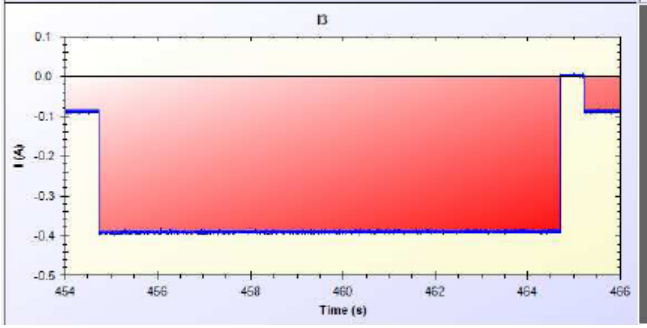
(1) See ARQUIMEA's high power distribution, control and monitoring ASIC(smart power) presentation on AMICSA 2010 proceedings

RADIATION NON CONFORMANCE

- SEL tests showed a LET threshold of 22.5 MeV cm mg^2 cm^{-1} 
- The latch-up was not destructive since the current was limited to 400mA.







400 to 500 s range
SEL enlarged

Sustaining time is 10s

Off time is 0.5s

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RADIATION NON CONFORMANCE (ANALYSIS)

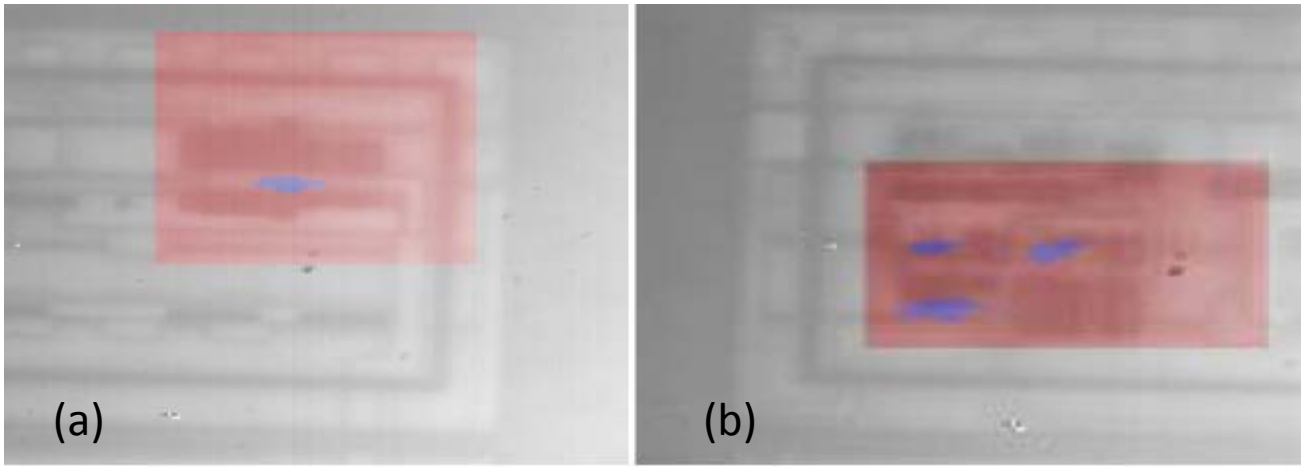
- An analysis on the radiation hardening techniques to avoid SEL in the core design was held and no issue was identified.

- Attention was then paid on the digital I/O pads which had not been modified for Latch Up immunity

- The Digital I/O pads had an enable circuitry where the PMOS and NMOS transistors were not isolated.

RADIATION NON CONFORMANCE (TESTS)

➢ Laser tests confirmed the hypothesis: The LU sensitive areas were located in the digital I/O Pads, the rest of the core was LU free



LU sensitive structures detected during laser scan on Input (a) and Output (b) pads

RADIATION NON CONFORMANCE (PAD MODIFICATION)

- The digital I/O PADS had to be modified to make them LU free
- Several options were evaluated and considered between ESA, ON-SEMI and ARQUIMEA
- The chosen solution only required a metal masks fix
- Fortunately some back-up lots were left at metal mask level at the foundry

ANALOG ASIC RUN 2

- Run 2 with the metal mask fix was fabricated from the back-up lot

- However…Things happen.

ANALOG ASIC RUN 2 (BODY FACTOR)

➢ It turned out that the body factor of the P channel 10x10 was too high in the back up lot. (the body factor is a process parameter out of the designer control).

➢In order to validate the lot:

1. Simulations were performed with a corner that reproduced the body factor drift.
2. ESD test was performed at two wafers and one wafer was sawed and some dice was assembled to be electrically tested.

➢At the same time some of the encapsulated dies were prepared for radiation test to see if the Latch up sensitivity improved or not

ANALOG ASIC RUN 2 (SEL INMUNITY)

- Latch Up test showed that the RUN 2 of the ASIC was Latch up free at least up to 67.5 MeV cm^2/mg

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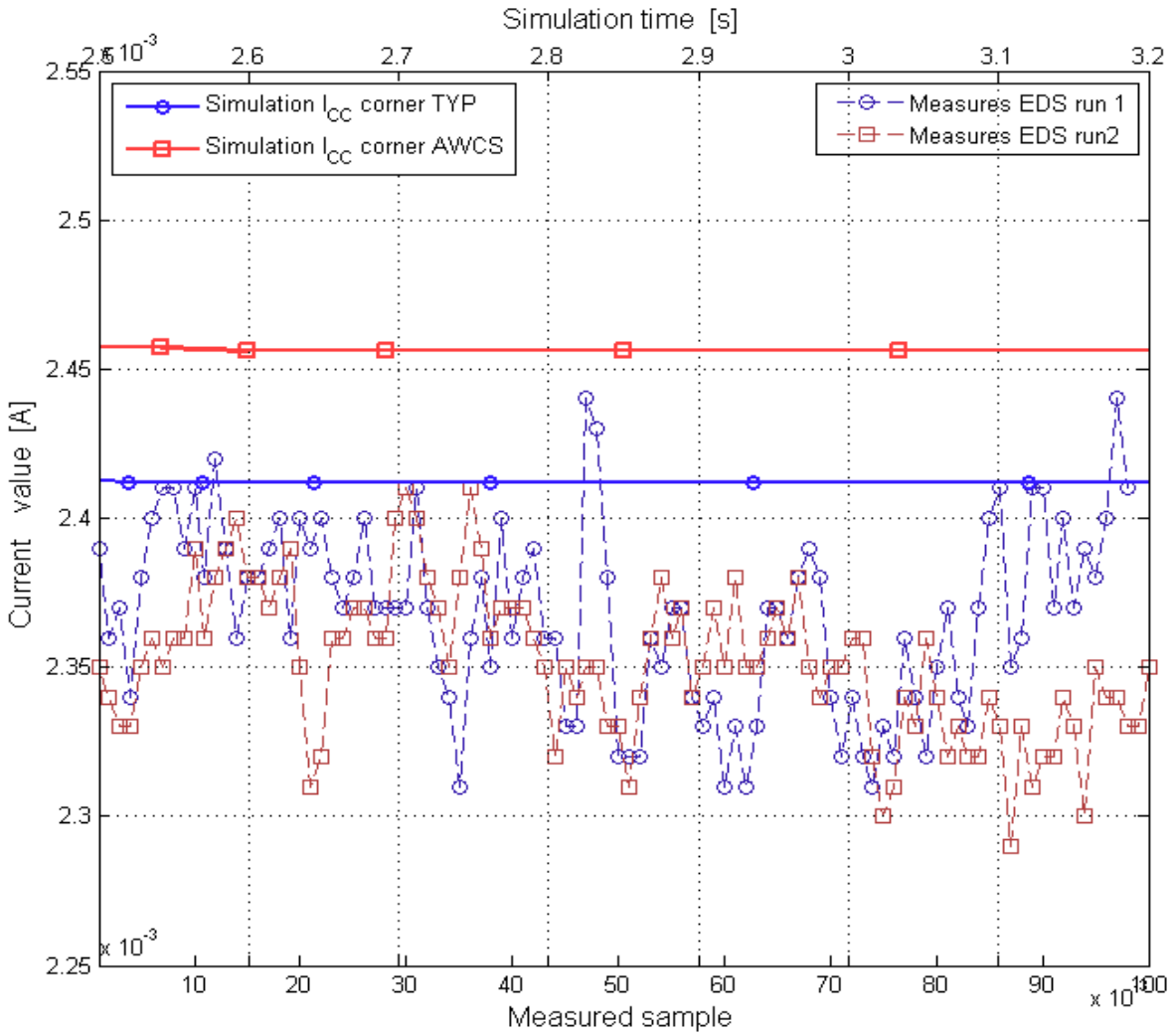
SIMULATION VS VALIDATION (ICC)



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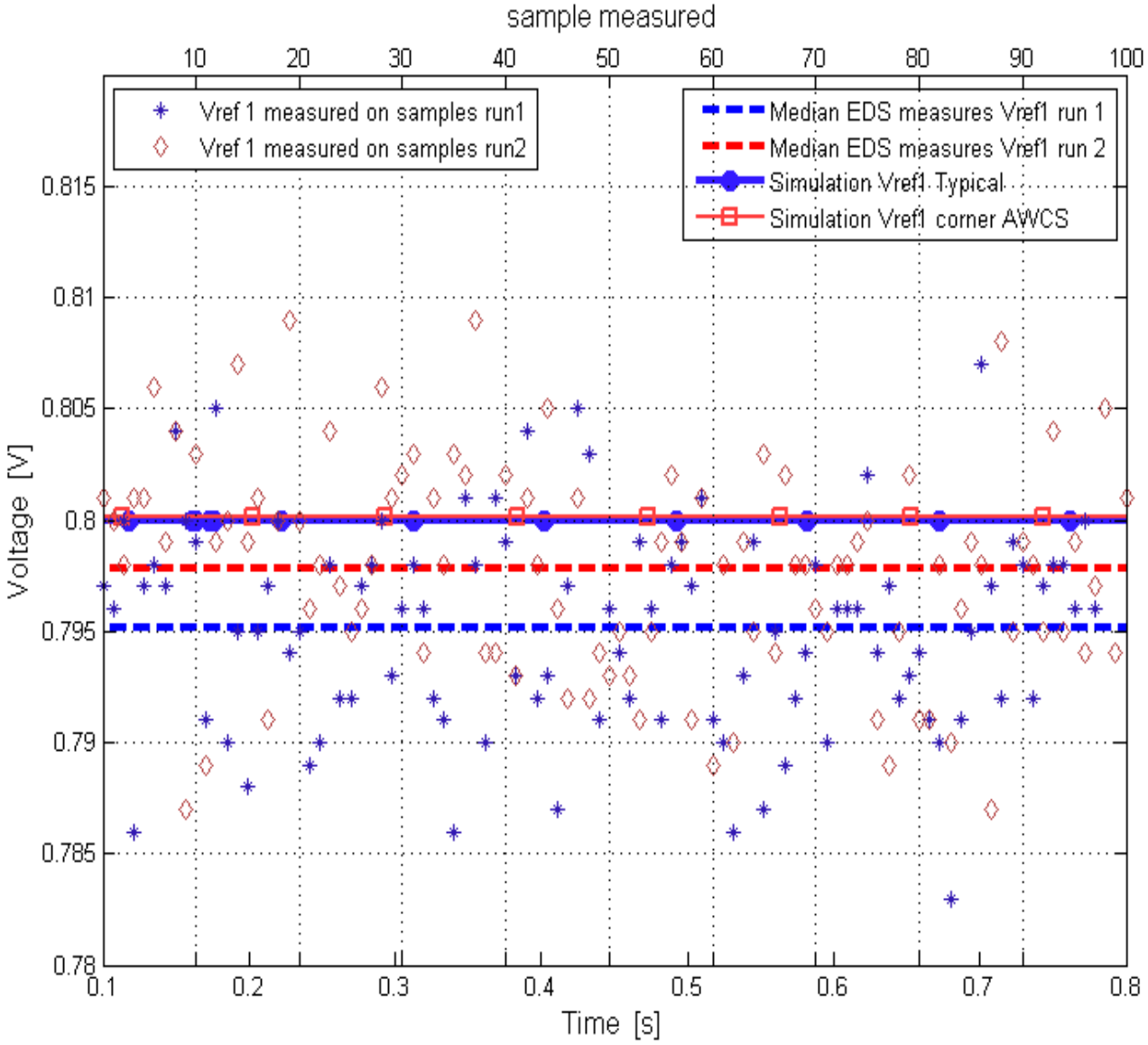
SIMULATION VS VALIDATION (VREF1)



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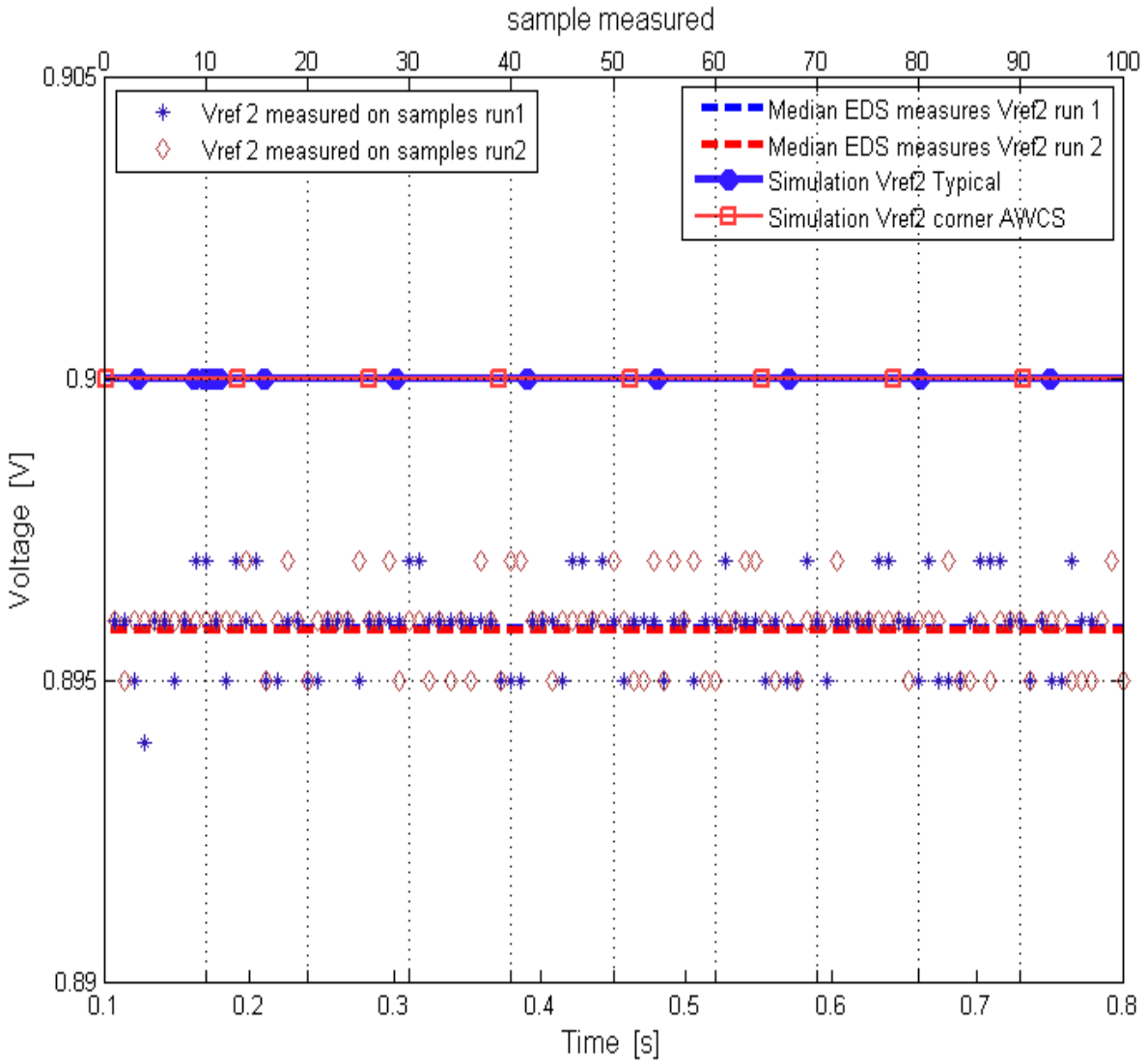
SIMULATION VS VALIDATION (VREF2)



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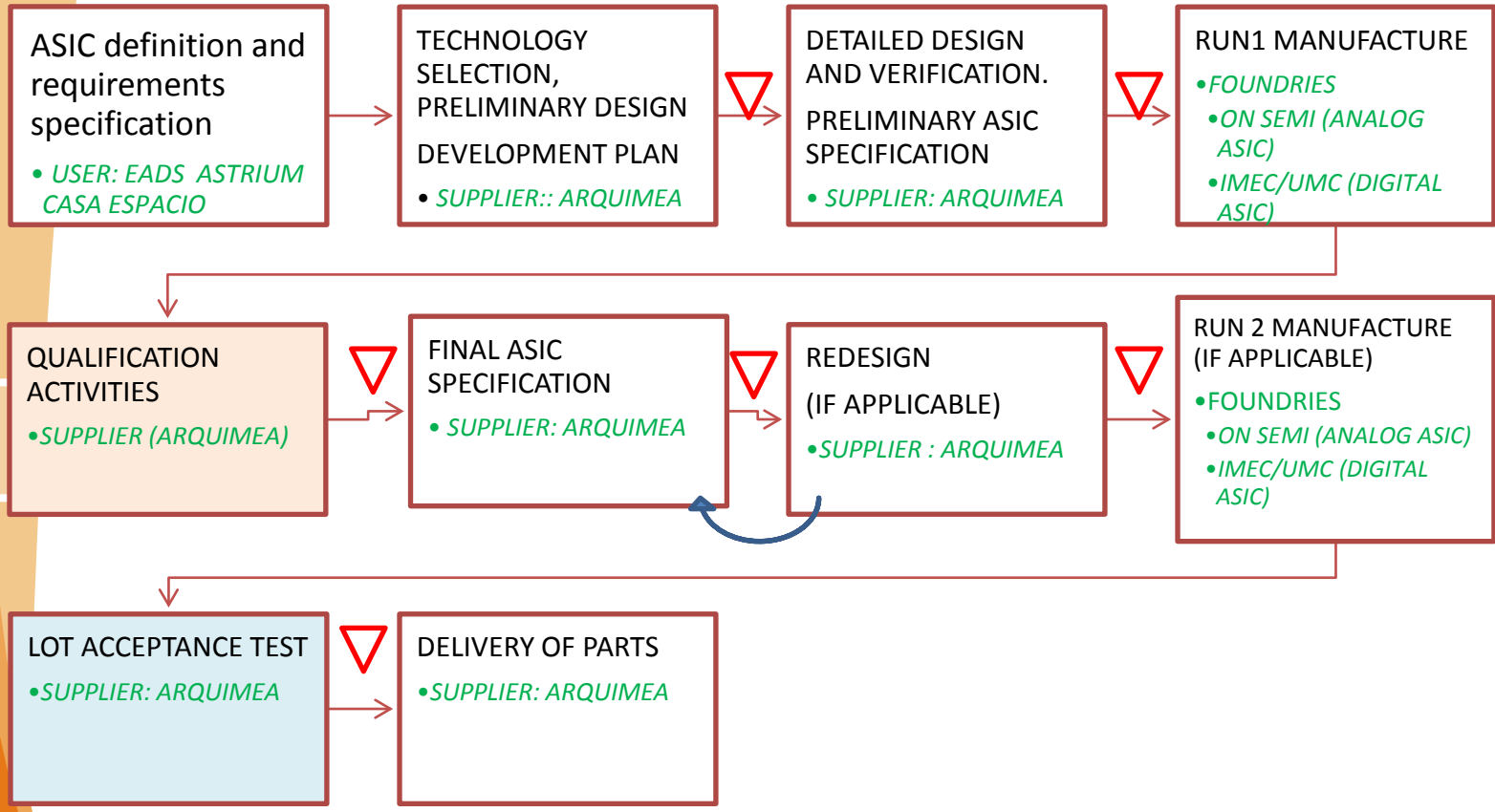
SUPPLY CHAIN



▽ Approvals
▪ *Responsible*

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QUALIFICATION FLOW OF ASIC DICE FOR HYBRID ASSEMBLY (ON RUN 1)

ON WAFER TEST
- *TEST HOUSE: IMS FRAUNHOFER*

DICE SELECTION AND CLASSIFICATION
- *USER: ECE*
- *SUPPLIER :ARQUIMEA*

▽

WAFER SAWING/DICING
- *TEST HOUSE: IMS FRAUNHOFER*

QUALIFICATION LOT ASSEMBLY (DICE RELATED TESTS)
- *ASSEMBLY HOUSE: INDRA*

PRECAP INSPECTION
- *. SUPPLIER: ARQUIMEA AND USER . ECE*

ASSEMBLY CAPABILITY TEST (BOND PULL & DIE SHEAR)
- *ASSEMBLY HOUSE: INDRA*

DICE FOR HYBRID QUALIFICATION*

* IN CASE OF SUCCESFULL QUALIFICATION OF RUN 1

SCREENING (SEM, ESD, ELECT. CHARACTER., BURN-IN, SEAL TEST).
- *TEST HOUSE: HIREX*

RADIATION TEST (TID, SEE)
- *TEST HOUSE HIREX*

THERMASL CYCLING AND POST TEST ASSEMBLY QUALITY EVALUATION
- *TEST HOUSE : HIREX*

DICE FOR FLIGHT* (HYBRID ASSEMBLY)

* IN CASE OF SUCCESFULL QUALIFICATION OF RUN 1

RELIABILITY TEST (2000 H LIFE TEST)
- *TEST HOUSE: HIREX*

▽

FAILURE ANALYSIS (IF APPLICABLE)
- *TEST HOUSE (HIREX)*

▽

▽ Approvals
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LOT ACCEPTANCE FLOW OF ASIC DICE FOR HYBRID ASSEMBLY (ON RUN 2, IF APPLICABLE)

ON WAFER TEST
- *TEST HOUSE: IMS FRAUNHOFER*

DICE SELECTION AND CLASSIFICATION
- *USER: ECE*
- *SUPPLIER :ARQUIMEA*

▽

WAFER SAWING/DICING
- *TEST HOUSE: IMS FRAUNHOFER*

LAT LOT ASSEMBLY (DICE RELATED TESTS)
- *ASSEMBLY HOUSE: INDRA*

PRECAP INSPECTION
- *. SUPPLIER: ARQUIMEA AND USER . ECE*

ASSEMBLY CAPABILITY TEST 1 (BOND PULL & DIE SHEAR)
- *ASSEMBLY HOUSE: INDRA*

DICE FOR HYBRID QUALIFICATION*

* IN CASE OF SUCCESFULL LAT OF RUN 2

SCREENING (SEM, ESD, ELECT. CHARACTER., BURN-IN, SEAL TEST).
- *TEST HOUSE: HIREX*

RADIATION TEST (TID, SEE) - DELTA
- *TEST HOUSE HIREX*

RELIABILITY TEST (1000 H LIFE TEST)
- *TEST HOUSE: HIREX*

▽

DICE FOR FLIGHT* (HYBRID ASSEMBLY)

* IN CASE OF SUCCESFULL LAT OF RUN 2

FAILURE ANALYSIS (IF APPLICABLE)
- *TEST HOUSE (HIREX)*

▽

▽ Approvals
- *Responsible*

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Acknowledgements

EADS-CASA ESPACIO

ESA

ON SEMICONDUCTORS (Support)

UC3M (Digital ASIC design)

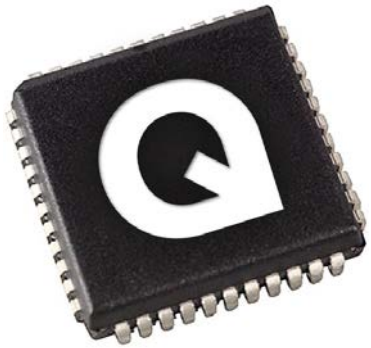
IMEC (Digital Backend and fabrication)

HIREX (Testing)

IMS FRAUNHOFER (On wafer Tests)

INDRA (Samples packaging)

And thank you for your attention!



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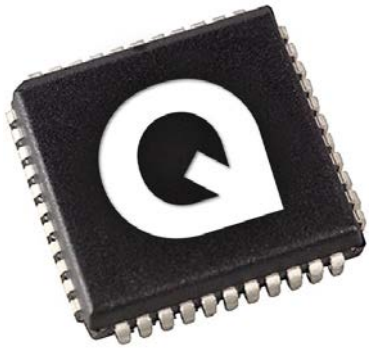

ARQUIMEA PARTICIPATES IN

APOLO DEVELOPING RADIATION HARDENING TECHNIQUES

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