# Integrated SAR Receiver/Converter for L, C and X-Bands

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## 1 INTRODUCTION

The receiver circuit described in this paper is intended for X (9.65 GHz), C (5.41 GHz) or L-band (1.2575 GHz) synthetic aperture radar (SAR) receiver. The circuit includes all the front end excluding the first low noise amplifier (LNA). In the planned application the LNA, together with band pass filters, is a separate circuit. However, the circuit in this paper can also be used as a stand-alone front end in less demanding applications by using its buffer amplifier as the LNA.

The circuit is a direct conversion receiver circuit consisting of three parallel signal channels, one for each band. The channels are further divided into quadrature I/Q branches. Every channel consists of an input buffer amplifier, and for each I or Q branch a down conversion mixer, a baseband filter and an analogue-digital (AD) converter. The band is hard selected. The bandwidth can be selected between 320 and 100 MHz. The AD converter has 8-bit, 7-bit, 6-bit, and 5-bit accuracy options. The circuit has single-sided inputs for RF and differential inputs local oscillator (LO) signals, except single-sided for L-band and 8-bit parallel LVDS-compliant output for digital data for each branch (I & Q). The interfaces parallel I/Q Data out, as well as the Test out/in, are multiplexed between the channels (bands) according to the band selection. The input buffer can be grounded during radar transmittance. The input matching is external. Unused inputs can be grounded. The process selected was ST 130 nm CMOS.

The circuit uses an external 440 MHz low jitter reference clock. There is also a clock output for synchronizing several parallel circuits. The block diagram of the circuit is in Figure 1.

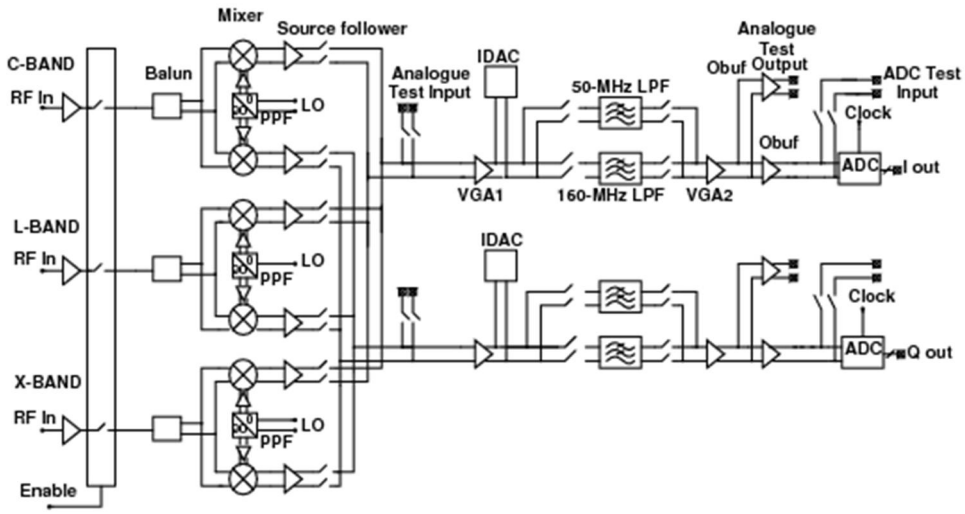


Fig. 1. Block diagram of the circuit. PPF = poly-phase filter and IDAC = current-steering D/A converter.

## 2 CIRCUIT DESIGN

### 2.1 RF front end

The architecture of the direct conversion receiver's front end is shown in Fig. 1. The RF front end consists of an amplifier, an active balun, two Gilbert cell mixers and a passive polyphase filter for the local oscillator signal. In order to prevent the overloading due to the transmit signal, there is two controlled attenuators in the signal path. The first is after the amplifier and the second is after the mixers. The wideband amplifier design is based on splitting-load inductive peaking technique [1]. The circuit is very simple consisting of inverter stages with resistive feedback, Fig. 2. The resistive feedback sets the gain and stabilizes the operating point of the stage. Inductive series peaking of amplifier stages is a well known trick to widen the bandwidth. In this modification the peaking inductor is placed at the gate of the NMOS transistor, whereas the signal is directly connected to the gate of PMOS transistor. Now the dominant pole is determined only by the gate-source capacitance of the NMOS transistor and the inductor instead of capacitance of both transistors and the inductor. Three stages are necessary and using low-area inductors from the design kit the chip area can be kept reasonable. Simulations show that even the whole band could be covered by a proper design. However, it is more feasible two cover X- and C-band with one design and L-band with its own design, where the inductors are not needed to widen the bandwidth.

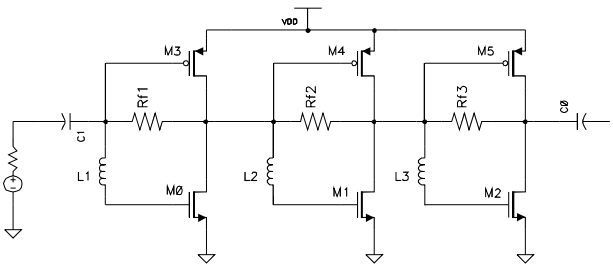


Fig. 2. Wideband amplifier schematic.

It turned out to be feasible to have separate RF circuits for each frequency band to avoid complex switching arrangement due to the different polyphase filters. In addition, due to the selectable baseband filters there will be switches between the front end and baseband circuits in any case. The LO baluns were external except for L-band LO an internal circuit which is depicted in [2]. It was decided to carry out the quadrature generation by passive polyphase filter in the local oscillator path. The polyphase filter offers two advantages, namely operation is at a single frequency and the amplitude unbalance is suppressed to some extent. The passive polyphase filter consists of resistors and capacitors, and is therefore sensitive to process variations. Using a stagger-tuned second order filter the errors are kept at insignificant level. Note that in theory the phase balance of the chosen topology is ideal (i.e. 90 degrees), and there is only amplitude unbalance.

A standard Gilbert-topology was chosen for the mixer. It is a wideband circuit especially suited for integrated circuit implementations. The performance is well known and balanced. With low supply voltage the stacked structure becomes inconvenient. In this design the balun can directly drive the RF-port transistors, and the separate current source can be omitted.

As the radar transmit signal might overload the receiver, a synchronized attenuator is needed. However, over 40 dB attenuation is difficult to achieve at one point on-the-chip. Power supply switching is the most effective approach, but has to be applied very smoothly to avoid transients from the switching itself. Therefore a signal path switch is designed between amplifier and balun. A second switching occurs before the baseband filters.

### 2.2 Analogue baseband circuit

The block diagram of the analogue baseband circuit is shown in Figure 1. It consists of a source follower designed to drive a large parasitic capacitive load, two VGAs (VGA 1 and VGA2), a 5th-order 160-MHz and 5th-order 50-MHz low-pass filter, an output buffer designed to drive the following 8-bit ADC, and an analogue test output.

The analogue baseband chain includes two variable gain amplifiers, VGA1 and VGA2. Both of them are wideband amplifiers (bandwidth > 1 GHz). The $5^{th}$-order low-pass filter, shown in Fig. 3, has been realized with a pseudo-differential gm-C technique because of the large 160-MHz bandwidth requirement and low 1.2-V supply voltage.

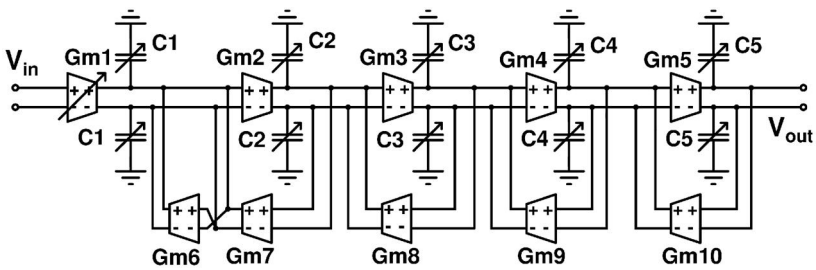


Fig. 3. Fifth-order gm-C low-pass filter.

The conventional approach to designing gm-C filters is to realize the transconductors with a wide bandwidth and high DC gain, thus mitigating their effect on the filter frequency response. However, it is generally difficult to implement a transconductor having both a wide bandwidth and a high DC gain simultaneously. This trade-off is further exacerbated by the very low supply voltage of the used deep-submicron CMOS technology. Therefore, the approach in this design is to accept a low DC gain for the transconductors, but to take the loss into account already in the filter synthesis [3],[4],[5]. The low DC gain enables the use of a simple transconductor circuit, which has no internal bandwidth limitation. All transconductors in the filter are designed to have a nominal 26-dB DC gain of which process variations are controlled by a negative resistance circuit. The corner frequency of the realized 5th-order gm-C filter is digitally controlled with 5-bit switched capacitor matrices.

In order to achieve fast start-up operation, DC offset compensation is realized with a 9-bit current-steering digital-to-analog converter (IDAC) Fig. 1. The designed 9-bit IDAC consists of an IDAC core and an output stage. The core includes nine binary-weighted PMOS current sources and a current-steering array constructed from nine digitally controlled binary-weighted PMOS switch pairs. The output stage consists of two NMOS current mirrors and a common-mode control circuit that is needed to set the desired 700-mV DC common-mode voltage at the IDAC output.

### 2.3 Analog-digital converter

The analogue-to-digital converter (ADC) circuit consists of a sample and hold (SH) front-end, six switched capacitor (SC) double-sampling 1.5-bit pipeline stages, and a 2-bit flash back-end stage, as shown in Figure 4. Double-sampling is utilized in the S/H and the MDACs to achieve a sampling rate of 440 MS/s with a 220 MHz clock. The clocks are derived from a small-amplitude 440 MHz sinusoidal signal by a two-stage clock amplifier and cross-coupled inverters. Redundant sign digit (RSD) correction is utilized to correct offsets of the comparators. The RSD logic circuit is a simple digital adder. Resolution of the ADC (from 5 to 8 bits) can be selected with a 2-bit control word.

The output data and clock are taken out by utilizing low-voltage differential signalling (LVDS) drivers.

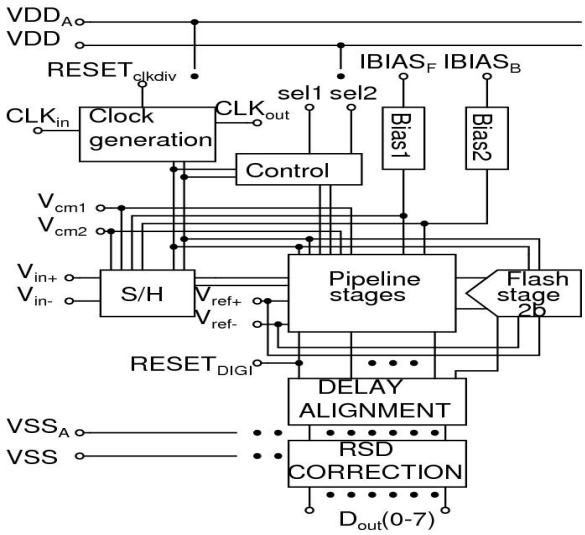


Fig. 4. Block diagram of the analogue-to-digital converter.

## 3 MEASUREMENT RESULTS

The circuit was processed with STM 130 nm CMOS process via CMP MPW service. There were three different measurement boards, one for each band. Figure 11 displays the test board; in this case C-band but the others are similar in appearance in this scale. L-band was measured in three different temperature from 0ºC to 45ºC, and C-band in five temperatures from -25ºC to +70ºC. X-band was measured in room temperature only. Figure 5 shows the C-band gain temperature dependence and gain adjustment range.

The LO to RF leakage values for different bands were: L-band -36.5 dB (single ended), C-band -35 dB (differential) and X-band -30 dB (differential). The RF and LO pads were all on one side of the chip. This forces to long parallel RF and LO lines on the test board and parallel bond wires, causing much cross-coupling. By comparing L-band (single ended) and C-band (differential) isolation one can see that a differential input helps quite a lot, but not enough to get acceptable isolation with the higher frequencies The LO leakage caused a large dc-offset, which limited considerably the usable range of the control settings, e.g. the gain adjustment, see Figure 5. The dc offset compensation range was not wide enough to compensate the generated offset in all temperatures.

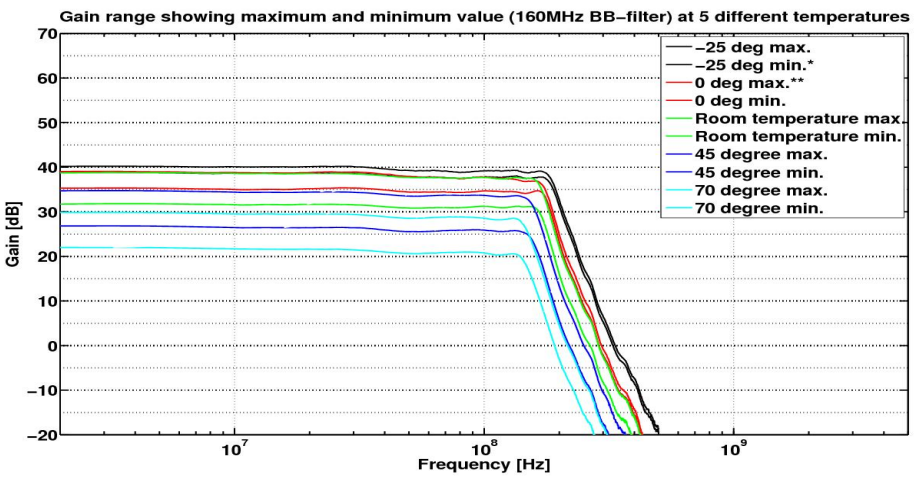


Fig.5 Gain and gain adjustment range of the 160MHz BB-filter at 5 different temperatures**.**

Alias signal suppression and gain flatness are shown for C-band in room temperature in Figures 6a and 6b below. The flatness is 1.2 and 1.5 dB, respectively. The worst case swing was with highest measured temperature and was (for all band widths) L-band 2.0 dB (+45°C) and C-band 2.3 dB (+70°C)

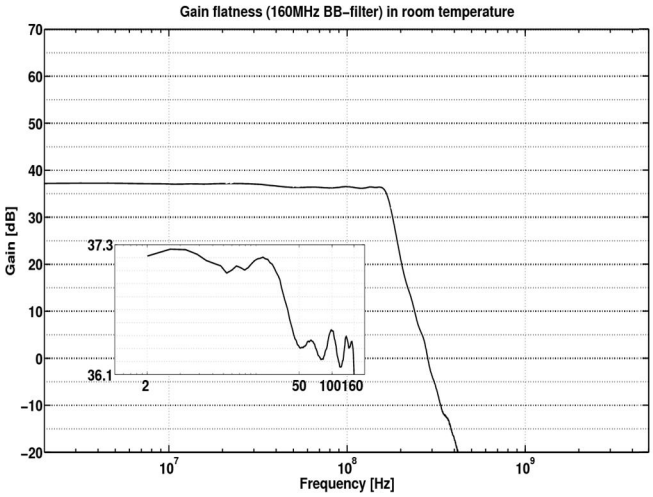


Fig. 6a. Gain flatness of 160MHz bandwidth in room temperature.

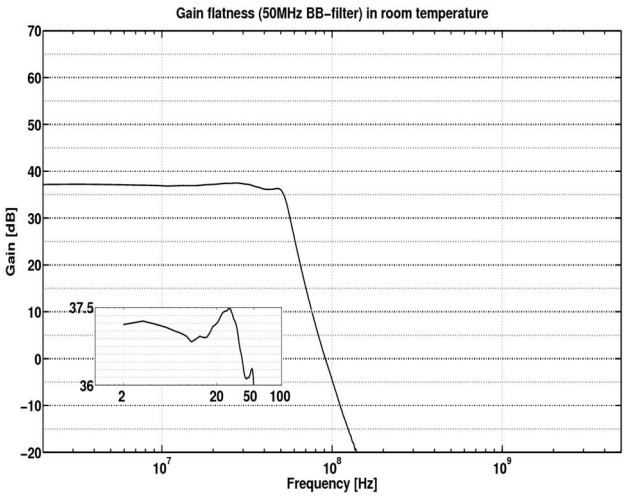


Fig. 6b. Gain flatness of 50MHz bandwidth in room temperature.

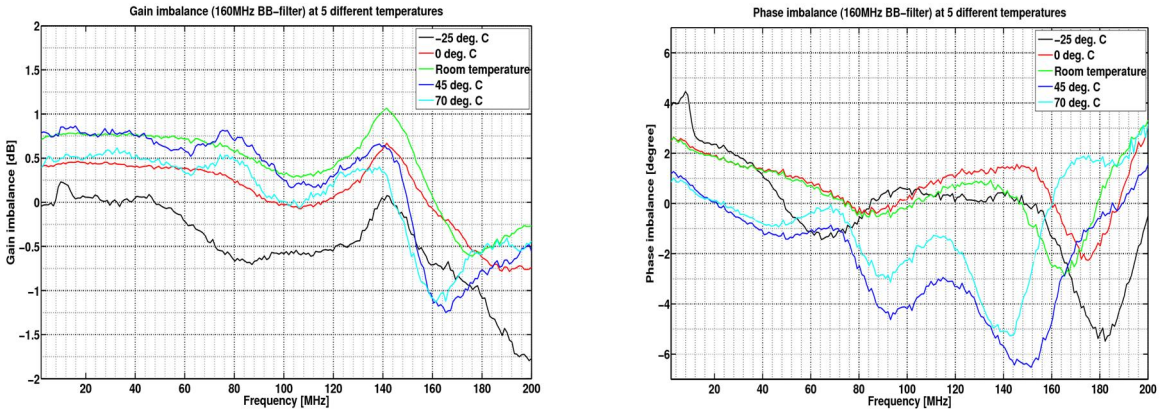


Fig. 7. Measured a) gain and b) phase imbalance of C-band in different temperatures.

Figure 7. displays the gain and phase imbalance of C-band in different temperatures. The gain imbalance is within ±0.5 dB except near the corner frequency (>140 MHz). The phase imbalance increases with the temperature being ±2.5° at room temperature and below and increasing to ±6° at +70°C.

Noise figure (NF) was strongly depending on the LO level. A level of LO + 5.5 dBm was defined as nominal and used in all the standard measurements defined in the measurement program. Figure 9 shows the C-band noise figure with 160 MHz band width as a function of the LO level. The highest level that could be driven without saturation was 6.5 dBm.

Other L-band and C-band parameters are summarized in Table 1.

It turned out that the X-band could not be measured properly. A test block of X-band RF frond end showed 14 dB less conversion gain that the L- and C-bands (being 20 and 22 dB), but was otherwise working properly, see Figure 10. When it was integrated with the whole circuit in the final version, the gain started to drop steeply after C-band frequency, Figure 8.

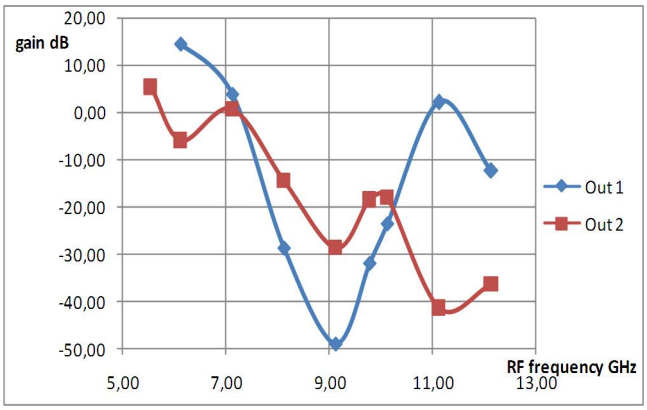


Fig. 8. Wide band measurement of the total gain. The circuit was matched to X-band. Matched L- and C-band total gains were in the order of 40 dB. Out1 is the initial test board result and Out 2 after re-tuning the matching.

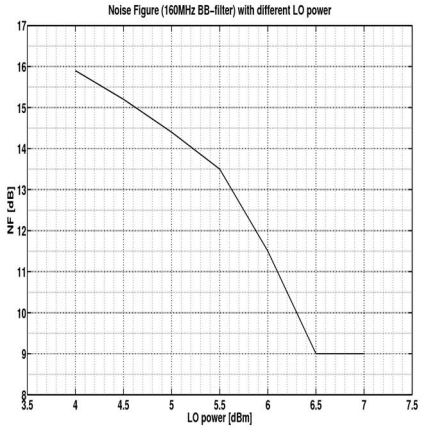


Fig. 9. Receiver noise figure vs LO power with 160MHz-BB filter

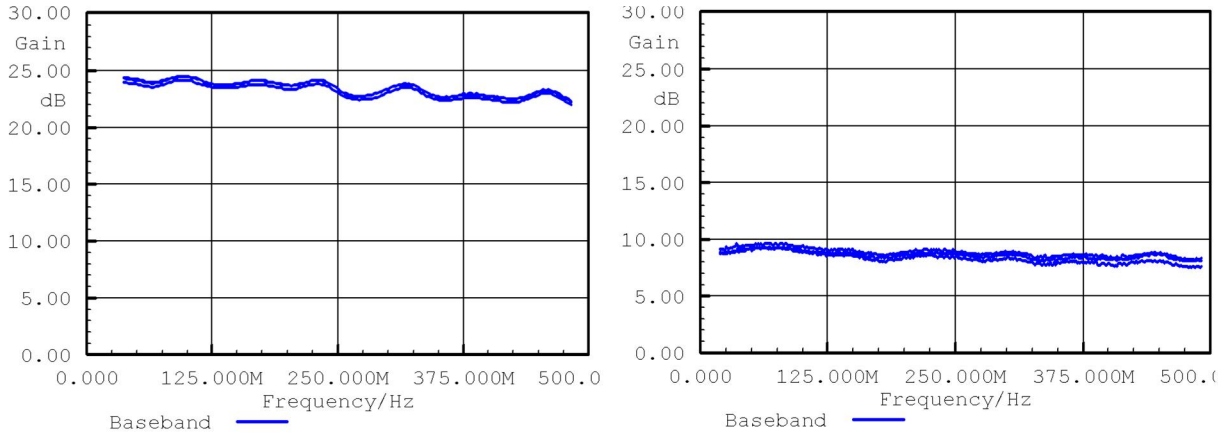


Fig. 10. Conversion gain of a) C-band and b) X-band measured from rf test block.

Several hypotheses were formed for the loss of X-band performance in the integrated version: on-chip inductor resonance, compression/saturation of signal, faulty design/layout, high losses on test board, faulty bondings. However, none of these hypotheses could be confirmed with additional measurements on the prototype chips and on the test structures and blocks processed separately before the final integrated version. The confirmation of the real reason would thus need processing of additional test circuits.

Table 1 Summary of the chip performance, compared to the ESA specifications.

| Name | Final ESA specifications | Compliance (over the temperature range unless otherwise stated) |
|---|---|---|
| LO power | < 7 dBm | < 6.5 dBm, before compression. |
| NF within Bandwidth | < 10 dB | L-band 320 MHz ≤ 11 dB; 100 MHz ≤ 15 dB ≤ 22°C; LO 5.5 dBm<br>C-band 320 MHz 9 dB at T 22°C, LO 6.5 dBm<br>C-band 320 MHz ≤ 13.5 dB; 100 MHz ≤ 18 dB ≤ 22°C; LO 5.5 dBm |
| Gain Flatness vs. Bandwidth | ±1.5 dB<br>Goal ±0.5 dB | C-band 2.3 dB worst case<br>L-band 2.0 dB worst case |
| Phase linearity vs. BW | ±5 deg (TBC) | ±15 deg |
| DNL | ±0.5 LSB | Yes, ±0.38 LSB |
| INL | ±0.5 LSB | ±0.58 LSB |
| IMD | -60 dBc, at -15 dBFS, 8 bits | -50 dBc, at -15 dBFS, 8 bits |
| Max power consumption | 900 mW | max 800 mW (8 bits, 320 MHz) min 500 mW (5bits, 100 MHz) |
| I/Q gain balance | ±0.5 dB | C-band ±1.1 dB, L-band ±0.8 dB |
| I/Q phase balance | ±5 deg | C-band ±5 deg, L-band ±7 deg (both±2.5 deg to 280/80 MHz) |
| Alias signal suppression | >30 dB | Yes |
| Dynamic range | 39 dB | Yes, 39 dB 100 MHz both bands<br>320 MHz C-band 37 dB, L-band 38 dB |

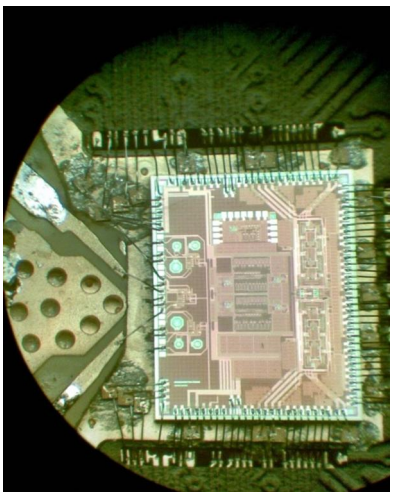

Fig. 10. The chip bonded on the test board (L-band connected).

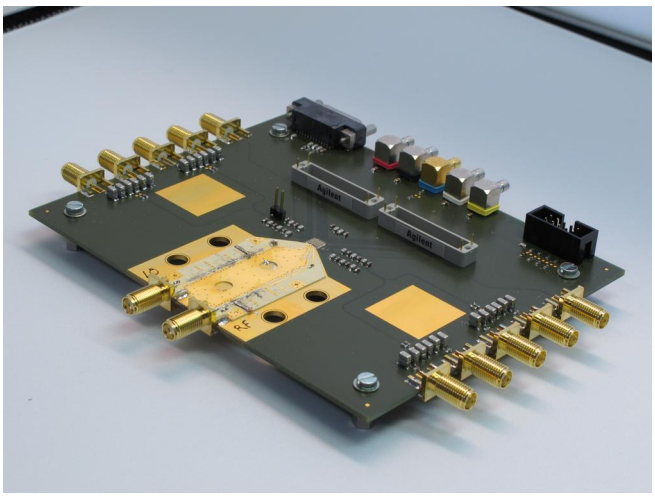

Fig. 11. Test board (C-band connected)

## 4 CONCLUSION

A multiband SAR receiver front end circuit from buffer amplifier (LNA separate) to ADCs was designed and realized. L and C-bands had the expected performance. X-band performance falls short of specifications because of insufficient gain in the RF stage. To achieve the desired gain at X-band either more amplifier stages are needed, or presumably, the design could be converted into a 130 nm BiCMOS process. The main shortcoming was the LO to RF leakage on the printed circuit board which caused large dc offset at the base band. This can be corrected only by changing the chip layout. Ways to reduce offset are: 1) to have differential LO feed for L-band, too, 2) to modify the layout to have LO feed orthogonal to RF for C and X-bands, or 3) to have a fractional frequency LO feed and frequency multipliers on-chip.

The performance of the baseband filter was expected. The main shortcoming was insufficient range in dc-offset compensation, at least with the LO leakage of the processed circuit. The ENOB of the ADC was adequate in 5-, 6- and 7-bit mode but was under expectations in 8-bit mode. The ENOB was noise limited, probably due to too small capacitors in sample and hold block, causing excess sampling noise.

All the controls are manual in the manufactured prototype. A production circuit would need automatic control loop designs for temperature compensation.

The size of the chip is 10.8 $mm^2$ and power consumption maximum (X-band, 320 MHz BW, 8-bit mode ADC) 800 mW. The chip size is pad-limited.

## References


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