150nm SOI – 77K Mixed-Signal Technology ATMEL

27-Aug-12

INTRODUCTION - 150NM SOI ATMEL TECHNOLOGY

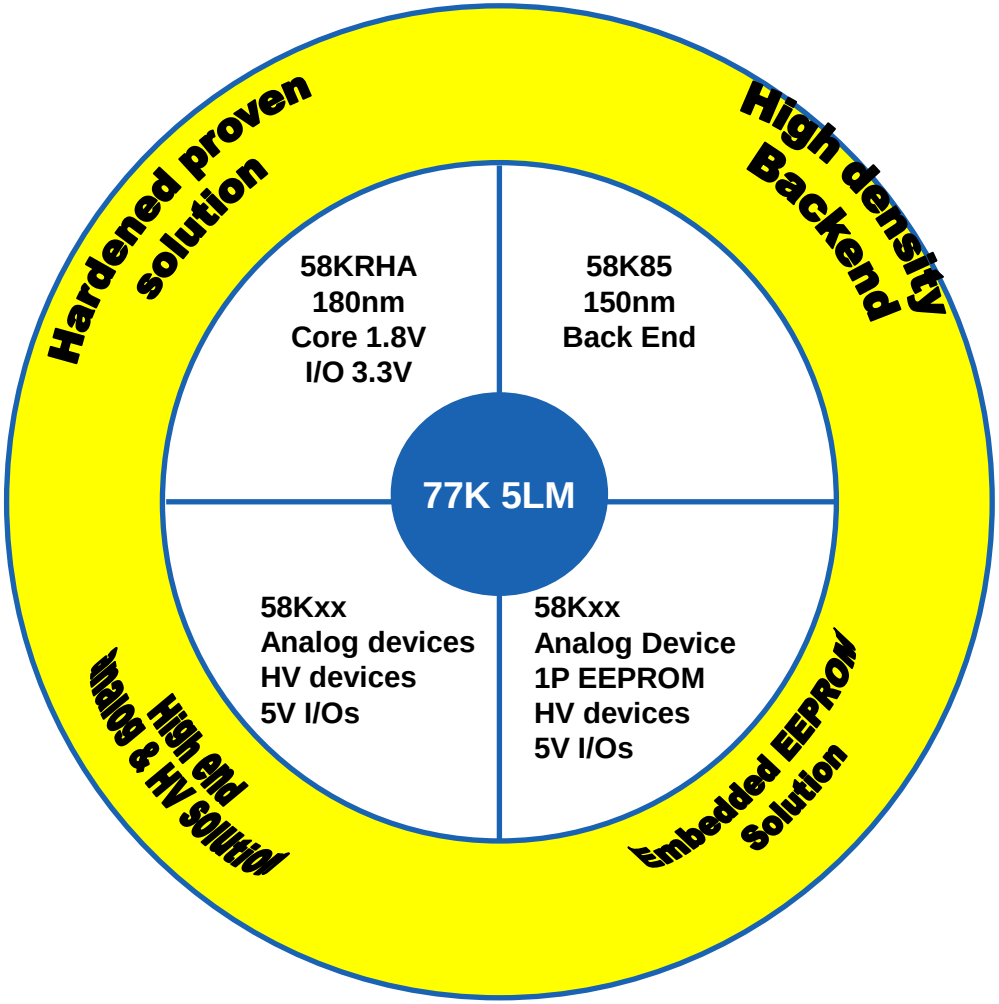
- For over 25years, ATMEL has been a leading supplier providing highly integrated solutions to the Aerospace Industry
- Use commercial, high volume, reliability proven process for Space
  - Basis from high runners
  - Follow Automotive and MicroControllers Business Unit
- 77K 150nm SOI Process qualification following MIL and ESCC standards
- Mixed-signal solutions target ASICS, ASSPs, mixed MicroControllers and SoC to miminize cost, area, power consumption
- Library Qualification with hi-rel and hardening solution is made in the military temperature range -55°C, 125°C
- SOI interesting capability for SEL immune process capability

Space targeted Technology with NVM

NODE	150 nm		110 nm	90 nm
TECHNONAME	58.85K	77K SOI	63.7K	63.9K
MAIN TECHNOLOGY FUNCTION	Embedded Micro	ASIC	Stand-alone Flash	Embedded Micro
SUPPLY LV HV	 1.8V 3.3V	 1.8V 3.3V / 5V	 1.8V 3.3V / 5V	 1.2V - LL 3.3V
NVM ARCHITECTURE	EEPROM 2T	EEPROM 2T 2T Single Poly	FLASH NOR 1T	FLASH NOR 1T
PART ID	AT69170E THEMIS	ASICs	AT69192E HYPNOS	-
STRENGTH	Density (up to 4Mb) Large library Logic RHBD proven from from ATC18RHA	Low process complexity (with single poly) Logic RHBD proven from ATC18RHA	Density (up to 32Mb) Prog time few us	Density (up to 32Mb) Prog time few us High speed read Optimized Power cunsumption

150nm Technology in 5LM on SOI

- Re-used process module and combined devices construction coming from commercial and Automotive technologies on same nodes



150NM SOI ATMEL TECHNOLOGY FEATURES

CMOS process	150nm Silicon On Insulator (SOI)
Core voltage	1.8V with Low Leakage option
Technology option	HV up to 120V, Mix-analog devices, 1Poly layer 1 Poly EEPROM block 32kB, HV >120V
Metal layers	AlCu, 5LM
Fab location	Lfoundry, France
Process status	Automotive qualification 2012
Packages	CGA, MQFP & high-pin-count packages
Pads	>900 counts, with double pad ring, Pad pitch 95µm
I/O's libraries supply	3.3V and 2.5V with 5V option (no 1.8V)
Others Options	Polyimide, Handle wafer contact, thick metal

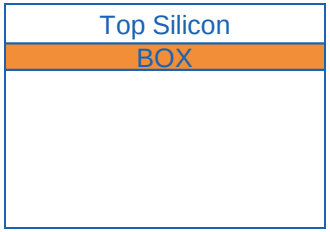
150NM SOI ATMEL TECHNOLOGY PROVEN SOLUTION

CMOS	MEMORY
❑ Core 1.8V and 3.3V re-used from ATC18RHA with proven hardening solution ❑ Back-end process flow re-used from AT58.85K (=AT69170E)with Metal1 pitch at 0.40um very agressive compared to competition ❑ 5V CMOS (optional) ❑ High Speed and low leakage option ❑ Logic 150kgate/mm2 (in 5LM)	❑ SRAM/DPRAM generator qual in MIL range as ATC18RHA ❑ Non Volatile Memory (1 poly EEPROM cell) coming from Automotive technologies 58.9/58.95K ❑ Poly fuses for Memory configuration or trimming
POWER DEVICES & ESD	**OTHERS DEVICES FOR MIX-SIGNAL**
❑ Full range of LDMOS 3.3V with low Rdson min. at 60 mW mm2 ❑ High level of latch up or SEL performance due to the Deep trench isolation and SOI substrate ❑ HV ESD proven structures from Automotive ❑ Thick power metallisation (8mOhm/sq)	❑ MIM capacitor ❑ Bipolar NPN/PNP transistors ❑ Zener Diodes ❑ Inductors ❑ High Capacitors ❑ High Poly resistors

AT77K CAPABILITIES VERSUS 58KRHA

- Same electrical characteristics based on 58K technology for Low Voltage 1.8V and 3.3V devices
  - Same minimum length ‘Lmin’ at 0.18µ on 1.8V devices
  - Same well, same implants and same thermal budget
  - Same oxide thickness for 1.8V and 3.3V devices

- Same top silicon final resistivity on substrate
  - SOI for 77K
    - Same top Silicon resistivity 3ohm.cm than 58KRHA Epi
    - 1.5µ of thickness
    - Buried oxide thickness = 1µ
  - No significant electrical influence (because deep SOI)



- Back-end Shrink from 58KRHA - 0.18µ to 77K - 0.15µ Design Rules
  - Possible gain of 25% of density on AT77K compared to AT58KRHA

- New additional options on 77K compared to AT58KRHA
  - Analog devices and HV LDMOS up to 80/120V
  - HV 5V I/Os
  - Single poly EEPROM
  - Deep Trench, Deep N-Well

77K Electrical performance versus AT58KRHA

- Simulation Model extraction
- SPICE model match between 77K and 58KRHA
- Any difference will be updated case by case if needed during qual period of time
- Below table gives the preliminary results
  - Simulation ATC18RHA: in black, acceptance range
  - Silicon measurement on AT77K: in black

1.8V Devices		NMOS 10/0.18	PMOS 10/0.18
Idlin (µA)	Simulation bcs / nom / wcs Measurement	1450 / 1280 / 1180 1266	-437 / -378 / -328 -345
Idsat (mA)	Simulation bcs / nom / wcs Measurement	6.87 / 6.03 / 5.29 5.58	-3.12 / -2.61 / -2.19 -2.29
Isub (pA)	Simulation bcs / nom / wcs Measurement	605 / 108 / 22 63	-665 / -108 / -22 -26
3.3V Devices		**NMOS ox3 10/0.36**	**PMOS ox3 10/0.36**
Idlin (µA)	Simulation bcs / nom / wcs Measurement	695 / 625 / 562 582	-274 / -214 / -185 -205
Idsat (mA)	Simulation bcs / nom / wcs Measurement	6.31 / 5.5 / 4.81 5.2	-3.35 / -2.8 / -2.35 -2.77
Isub (pA)	Simulation bcs / nom / wcs Measurement	23.86 / 6.95 / 4.23 12.9	-59 / -11 / -4.7 -17

CMOS 1.8V / 3.3V / 5V ELECTRICAL PERFORMANCE

MOS 1.8V (28A tox)

Device PDK name	Description	Model
nfet	1.8V (28A gate oxide) Std Vt NMOS	nmos
pfet	1.8V (28A gate oxide) Std Vt PMOS	pmos
nfethvt	1.8V (28A gate oxide) High Vt NMOS	nmoshvt
pfethvt	1.8V (28A gate oxide) High Vt PMOS	pmoshvt

MOS 3.3V (70A tox)

Device PDK name	Description	Model
nfetox3	3.3V (70A gate oxide) NMOS	nmosox3
pfetox3	3.3V (70A gate oxide) PMOS	pmosox3

MOS 5V (250A tox)

Device PDK name	Description	Model
nfetox5	5V (250A gate oxide) NMOS	nmosox5
nfetox5_nb	5V (250A gate oxide) NMOS incl. neighbouring box	nmosox5
pfetox5	5V (250A gate oxide) PMOS	pmosox5
pfetox5_nb	5V (250A gate oxide) PMOS incl. neighbouring box	pmosox5

8.1.1 LV MOS Logic devices, 1.8v (28A gate oxide)

Device Name	Model Name	Description	Min. Size (um)	Vt (Volt)	BVdss (Volt)
nfet	nmos	LV NMOS 1.8V	0.18	0.52	>2.0
pfet	pmos	LV PMOS 1.8V	0.18	-0.51	<-2.0
nfethvt	nmoshvt	High VT NMOS low leakage	0.18	0.66	>2.0
pfethvt	pmoshvt	High VT PMOS, low leakage	0.18	-0.65	<-2.0

Vt values given are for Lmin and W = 10um, measured with a linear extraction method.

8.1.2 MV MOS devices, 3.3v (70A gate oxide) and 5v (250A gate oxide)

Device Name	Model Name	Description	Min. Size (um)	Vt (Volt)	BVdss (Volt)
nfetox3	nmosox3	NMOS 3.3V	0.36	0.65	>3.6
pfetox3	pmosox3	PMOS 3.3V	0.36	-0.65	<-3.6
nfetox5	nmosox5	NMOS 5V	1	0.7	>5.5
pfetox5	pmosox5	PMOS 5V	1	-0.8	<-5.5
nfetox5_nb	nmosox5_nb	NMOS 5V with NB	1	0.7	>5.5
pfetox5_nb	pmosox5_nb	PMOS 5V with NB	1	-0.8	<-5.5

Vt values given are for Lmin and W = 10um, measured with a linear extraction method.

LDMOS ELECTRICAL PERFORMANCE

3.3V LDMOS (70A tox)

Device PDK name	Description	Model
ldnfet25_sbc	25V ldnmos source body closed	ldnmos25_sbc
ldnfet25_sbo	25V ldnmos source body open	ldnmos25_sbo
ldnfet45_sbc	45V ldnmos source body closed	ldnmos45_sbc
ldnfet45_sbo	45V ldnmos source body open	ldnmos45_sbo
ldnfet65_sbc	65V ldnmos source body closed	ldnmos65_sbc
ldnfet65_sbo	65V ldnmos source body open	ldnmos65_sbo
ldnfet80_sbc	80V ldnmos source body closed	ldnmos80_sbc
ldnfet80_sbo	80V ldnmos source body open	ldnmos80_sbo
ldnfet120_sbc	120V ldnmos source body closed	ldnmos120_sbc
ldnfet120_sbo	120V ldnmos source body open	ldnmos120_sbo
ldpfet25_sbc	25V ldpmos source body closed	ldpmos25_sbc
ldpfet25_sbo	25V ldpmos source body open	ldpmos25_sbo
ldpfet45_sbc	45V ldpmos source body closed	ldpmos45_sbc
ldpfet45_sbo	45V ldpmos source body open	ldpmos45_sbo
ldpfet65_sbc	65V ldpmos source body closed	ldpmos65_sbc
ldpfet65_sbo	65V ldpmos source body open	ldpmos65_sbo
ldpfet80_sbc	80V ldpmos source body closed	ldpmos80_sbc
ldpfet80_sbo	80V ldpmos source body open	ldpmos80_sbo
ldpfet120_sbc	120V ldpmos source body closed	ldpmos120_sbc
ldpfet120_sbo	120V ldpmos source body open	ldpmos120_sbo

Type	Source-Body open (SBO)	Source-Body close (SBC)	RDSon*A *1 [Ω*mm²]	IDSAT/W *2 [µA/µm]	RDSon*W [kΩ*µm]
3.3V LDNMOS (70A Gate Oxide)					
25V	ldnfet25_sbo	ldnfet25_sbc	0.047	tbd	11.9
45V	ldnfet45_sbo	ldnfet45_sbc	0.075	tbd	15.2
65V	ldnfet65_sbo	ldnfet65_sbc	0.091	tbd	16.7
80V	ldnfet80_sbo	ldnfet80_sbc	0.335	tbd	33.6
120V	ldnfet120_sbo	ldnfet120_sbc	tbd	tbd	tbd
5V LDNMOS (250A Gate Oxide)					
25V	ldnfet80ox5_sbo	ldnfet80ox5_sbc	tbd	tbd	tbd
45V	ldnfet120ox5_sbo	ldnfet120ox5_sbc	tbd	tbd	tbd
3.3V LDPMOS (70A Gate Oxide)					
25V	ldpfet25_sbo	ldpfet25_sbc	0.144	tbd	38.2
45V	ldpfet45_sbo	ldpfet45_sbc	0.300	tbd	55.8
65V	ldpfet65_sbo	ldpfet65_sbc	0.515	tbd	86.3
80V	ldpfet80_sbo	ldpfet80_sbc	0.671	tbd	96.3
120V	ldpfet120_sbo	ldpfet120_sbc	tbd	tbd	tbd
5V LDPMOS (250A Gate Oxide)					
25V	ldpfet80ox5_sbo	ldpfet80ox5_sbc	tbd	tbd	tbd
45V	ldpfet120ox5_sbo	ldpfet120ox5_sbc	tbd	tbd	tbd

OTHERS ELECTRICAL PERFORMANCE

Bipolar transistors

Device PDK name	Description	Model
lnpn	Lateral NPN transistor	
pnp_vert	Vertical PNP bipolar	pnp_vert

8.1.11 Bipolar

Device Name	Model Name	Description	Beta	Early Voltage (V)
pnp_vert	pnp_vert	PNP	2.5	25
lnpn	lnpn	Lateral NPN	tbd	tbd

Diodes

Device PDK name	Description	Model
dz_6p2_esd	6.2V Zener ESD diode	
dfreew_esd	80V freewheeling ESD diode	

8.1.10a Diodes

Device Name	Model Name	Description	Breakdown Voltage
dz_6p2_esd	dz_6p2_esd	Zener Diode	6.2 @ 10uAmp
dfreew_esd	dfreew_esd	Free Wheeling Diode	> 80

Capacitors

Device PDK name	Description	Model
moscap	1.8V MOS capacitor	cap_mos
moscapox3	3.3V MOS capacitor	cap_ox3
moscaphv	HV MOS capacitor	cap_moshv
momcap	Metal / Metal HV capacitor (BV>80V)	momcap
p2bncap	Poly2-Buried N+ capacitor	p2bncap
cmim	MIM capacitor (TM/TM-1)	cmim

8.1.9 (Oxide) Capacitances

Device Name	Model Name	Description	Optical Oxide Thickness (A)	Capacitance Value (fF/um2)	Max Voltage
moscap	cap_mos	Poly2 to LV N-Well (1.8V Oxide)	28	9.10	2
moscapox3	cap_mosox3	Poly2 to LV N-Well (3.3V Oxide)	70	4.5	3.6
moscaphv	cap_moshv	Poly2 to HV N-Well (Thick Oxide)	250	1.35	12
p2bncap	p2bncap	Poly2 to BN+ (Thick Oxide) [1)]	290	1.19	14
cmim	cmim	MIM capacitor	405	1.6	6
momcap	momcap	High Voltage capacitor	3600	0.48	120

BIPOLAR, DIODES, CAPACITOR ELECTRICAL PERFORMANCE

Bipolar transistors

Device PDK name	Description	Model
lnpn	Lateral NPN transistor	
pnp_vert	Vertical PNP bipolar	pnp_vert

8.1.11 Bipolar

Device Name	Model Name	Description	Beta	Early Voltage (V)
pnp_vert	pnp_vert	PNP	2.5	25
lnpn	lnpn	Lateral NPN	tbd	tbd

Diodes

Device PDK name	Description	Model
dz_6p2_esd	6.2V Zener ESD diode	
dfreew_esd	80V freewheeling ESD diode	

8.1.10a Diodes

Device Name	Model Name	Description	Breakdown Voltage
dz_6p2_esd	dz_6p2_esd	Zener Diode	6.2 @ 10uAmp
dfreew_esd	dfreew_esd	Free Wheeling Diode	> 80

Capacitors

Device PDK name	Description	Model
moscap	1.8V MOS capacitor	cap_mos
moscapox3	3.3V MOS capacitor	cap_ox3
moscaphv	HV MOS capacitor	cap_moshv
momcap	Metal / Metal HV capacitor (BV>80V)	momcap
p2bncap	Poly2-Buried N+ capacitor	p2bncap
cmim	MIM capacitor (TM/TM-1)	cmim

8.1.9 (Oxide) Capacitances

Device Name	Model Name	Description	Optical Oxide Thickness (A)	Capacitance Value (fF/um2)	Max Voltage
moscap	cap_mos	Poly2 to LV N-Well (1.8V Oxide)	28	9.10	2
moscapox3	cap_mosox3	Poly2 to LV N-Well (3.3V Oxide)	70	4.5	3.6
moscaphv	cap_moshv	Poly2 to HV N-Well (Thick Oxide)	250	1.35	12
p2bncap	p2bncap	Poly2 to BN+ (Thick Oxide) [1]	290	1.19	14
cmim	cmim	MIM capacitor	405	1.6	6
momcap	momcap	High Voltage capacitor	3600	0.48	120

RESISTORS, MEMORIES ELECTRICAL PERFORMANCE

Resistors

Device PDK name	Description	Model
rplow	Poly resistor (235 Ohm/sq)	rplow
rpolyhigh	Poly resistor (235 Ohm/sq)	rpolyhigh
rpolySH	Poly resistor (900 Ohm/sq)	rpolysh
rphigh	Poly resistor (900 Ohm/sq)	rpolysh

8.1.8 Resistors

Device Name	Model Name	Description	Unit	Target
rplow	rplow	Poly-2 Sheet Resistance	Ohm/sq	235
rpolyhigh	rpolyhigh	Poly-2 Sheet Resistance	Ohm/sq	235
rpolysh	rpolysh	Poly-2 Sheet Resistance	Ohm/sq	900
rphigh	rphigh	Poly-2 Sheet Resistance	Ohm/sq	900

Memory

Device PDK name	Description	Model
ee	Single Poly EEPROM	en
en	Sense	sn
sn	Select	sn
	Byte Select	nwmv

8.1.12 Memory

Device Name	Model Name	Description	Vt (V)	Area (um2)
ee	e2c_77k_on	Single Poly EEPROM – ON State	-2	5
	e2c_77k_off	Single Poly EEPROM – OFF State	2	

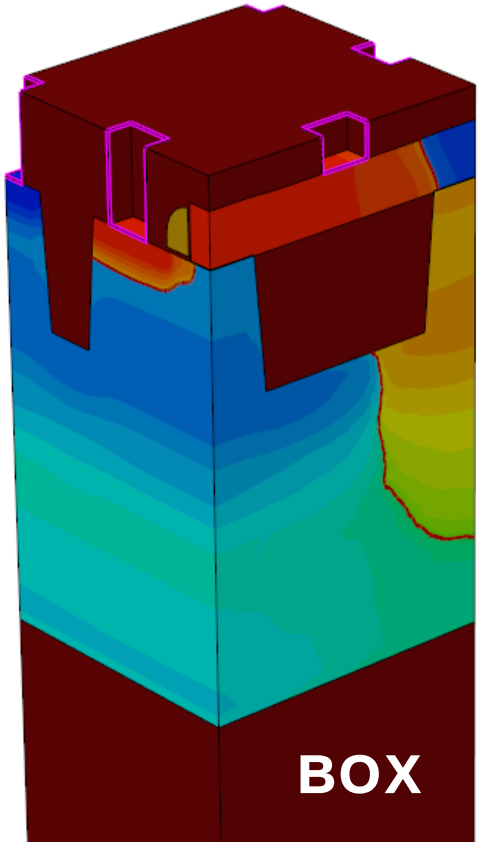
Device Name	Model Name	Description	L (um)	W (um)	Vt(V)	BVdss
sn	sn	Select	0.7	0.24	0.55	>13
en	en	Sense	0.7	0.24	0.25	>13
tbd	nmv	Byte select	1.4	0.74	0.75	>15.2

RADIATION HARDENING CAPABILITIES

- Evaluation of radiation capabilities will be completed by the end of 2012 according to MIL and ESCC standards on 2 Test Vehicles one for memories and one for others I/Os and Standard cell librray
- Rad hardness targets

  TID 300Krads @3.3V

  SEL >80 MeV/mg/cm2 @125°C

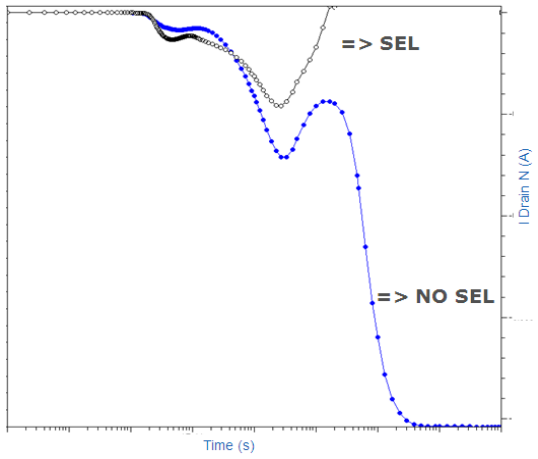


- SEL free managed with the use of the deep trench for MOS isolation but very high density lost (cell size increased by min. x1.4)
- SEL robustness assessment to be completed without isolation with current 150nm design rules
- DeepWell Option under development and R&D phase to be SEL free without using deep trench
- 3D TCAD simulation structures used to assess radiation characteristics (SEE and SEL) with/without BOX and with/without DeepWell

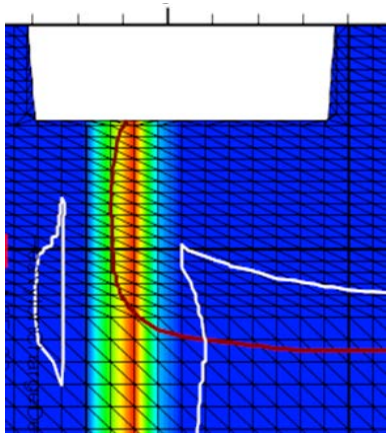
SEL TCAD SIMULATION 150NM SOI

Simulation used to assess design rules between body ties and diffusion N+/P+ area (Ltap) and N+ to P+ spacing (SAC) and adjust the best deepwell R&D conditions

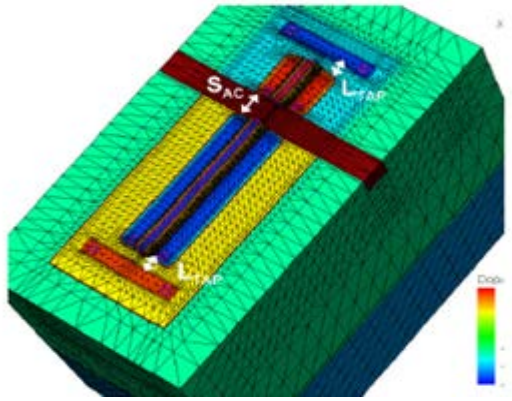
- Simulation are done on a Silicon Controlled Rectifier (SCR) structures in the worst case at Vccmax up to 145°C condition and configuration along the Nwell/Pwell junction
- The latch-up characterization is done by applying a positive current injection in the anode (P+ source)
- The latch-up is defined when the drain current remains to a high current for a given period of time otherwise drain current is recovered to zero when latch-up free



Latchup electrical characteristics



Cross-section with one ion stricke accross the Nwell/Pwell junction



3D inverters structures wih main Design rules assessed

Current result: no SEL at 145°C, 1.98V, LET=55MeV.cm²/mg wo DeepTrench & DeepNWell

PDK & DK RELEASE WIH LIBRARIES STATUS

First PDK & DK release on Prime alpha customer in Q4 2012

- PDK Based on Finesim simulator with Spectre models from CADENCE
- Physical layout verification done with Assura from Cadence including parasitic extraction
- First DK construction with the same package and view as ATC18RHA (Dkbuilder own AeroSpace builder solution)

Libraries

- Characterization done with SiliconSmart from Magma/Synopsis
- Re-built digital library from ATC18RHA (hardened lib available & charac)
- NVM up to 32 kbits (5k & 16kbytes unhardened block available)
- I/Os 5V (under construction)
- Very large analog catalog (unhardened libs available on-demand)

Hardened analog libraries

- Preliminary state of the art done with large publication by Vanderbilt with trade off in speed, consumption, area, maturity

Conclusion - 150NM SOI ATMEL TECHNOLOGY

- ASIC, ASSPs
- Analog as Full custom (End-User Design)
- RadHard proven Analog Library
- ATC18RHA Compatibility (simulation models)
- 5V IOs
- NVM
- Low power
- HV up to 60V
- Possibility of RF module in the future

PLANNING OF NEW 150nm ASIC/ASSP OFFERING

Phase 1:
Digital Lib Offering
Year 2012

- Tape-Out Done of TVs
- Ongoing Characterisation
- PDK for prime on Q4-2012
- End of Qual radiation and intrinsic reliability in Q4-2012

Phase2 :
Mix Signal Offering with I/Os 5V
Year 2013

- New SEC with unhardened analog libs
- First ASIC with custom analog solution
- Open to add HV, NVM, I/Os 5V Test chips

Rad Hard Analog Lib Offering
Year 2013/2014

Deep submicron (<=90nm mixed)