RADIATION HARDENED MIXED-SIGNAL IP WITH DARE TECHNOLOGY

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ABSTRACT

Recent trends show the growing need for more analog and mixed-signal IP to enhance the intelligence and reduce the cost of satellites. This paper presents the current state of the imec DARE solution with a focus on the strong increase in mixed-signal and analog IP blocks. In addition, the DARE solution is being extended to high-voltage technology targeting a similar mixed-signal IP offering in a different foundry technology. First the recent improvements and additions to the DARE library are presented. Secondly radiation test results on technology level are presented showing the extensive level of analogue characterization of the DARE solution. The mixed-signal expansion is illustrated with a software controlled SOC ASIC project. This ASIC contains, amongst others, improved, hardened PLL and ADC blocks. These blocks will be discussed together with the under-radiation simulation approach.

DARE+ ACTIVITY

The Design Against Radiation Effects (DARE) library is being further developed in the ESA activity DARE+. The focus of this follow-up activity is to strengthen the existing, mainly digitally oriented, UMC 180nm based offering and expand it with Mixed-Mode capabilities. Developments are ongoing to add a set of integrated clock gating cells, a Dual Port SRAM Compiler, improve the single event (SE) behavior of the existing Phase Locked Loop (PLL), extend the common mode input range of the available LVDS Receiver and improve the reliability and mixed-mode performance of the IO cells. All the library cells are re-characterized with the Mixed-Mode transistor models. Table 1 lists the DARE+ library activities.

DARE+ increases the analog content with a bandgap design and a linear voltage regulator. These analog circuits have been designed up to now with the standard provided transistor models and with the experience of good analog designers. However for advanced high-speed and high-accuracy designs an improved model is required. The Analog Design Kit (ADK) currently models the basic geometry effects of the Enclosed Layout Transistor (ELT), but it's the goal to also model Total Ionizing Dose (TID) effects for the analog components in the technology and further increase the simulation accuracy of analog transistor parameters. Table 2gives an overview of the selected analog components and the relevant analog parameters that are (possibly) influenced by TID.

Radiation tests are scheduled on a Devices Test Vehicle (DTV) that was designed and taped-out in Q1 2012. Transistors for many width and length combinations, with and without ELT geometry, inside or outside triple well, at 1.8V or 3.3V, … are used in test structures to measure IV-curves, VT-shift, matching, noise under different radiation conditions. The DTV is not intended for SEE measurements. Figure 2 shows the 5mm by 5mm die layout of the DTV. First test results are expected in Q3 2012.

Table 1 DARE+ library activities

Library Element:	Basic Specification:
Integrated Clock Gating Cells	X2, X4, X9 drive strength versions
Dual Port SRAM Compiler	New development
PLL	SE hardening with analog techniques in Voltage Controlled Oscillator (VCO) and Charge Pump (CP) Lower input frequency to 10MHz Divide by 8 or by 16 in feedback path
LVDS Receiver	Extended common mode input range: -4V to +5V
IO cells	Increase Simultaneous Switching Outputs (SSO) ratio Optimize Electrostatic Discharge Level (ESD) for 2kV Human Body Model (HBM)
Linear Voltage Regulator	Supply for small digital core Vin = 3.3V, Vout = 1.8V
Bandgap	Vout = 1.25V, Vsupply = 1.8V
All	Mixed-Mode characterization

Table 2 Analog active components and TID affected device parameters

Component type	Analog parameter
MOS transistors (1.8V, 3.3V, Low-VT, triple well, ELT, straight)	Leakage currents, VT-shift, noise, matching, mobility, breakdown voltage
Bipolar transistors (multiple emitter sizes)	Beta, noise, leakage current, mismatch, transit time
Diodes (multiple aspect ratios)	Reverse current, ideality factor, barrier potential

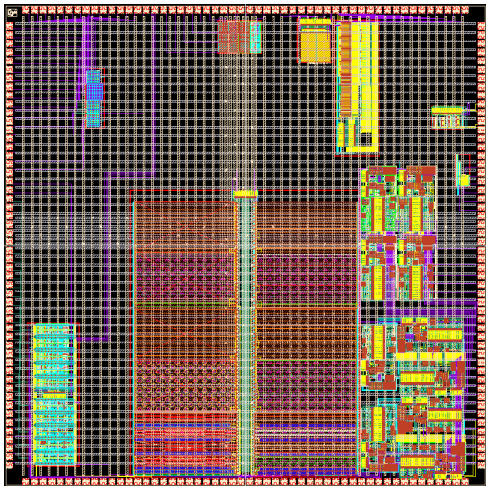

Figure 1 Layout view of DARE+ Devices Test Vehicle

DARE PORTING

The first steps have been taken to create a radiation hardened library in XFAB .18 technology, similar to the existing UMC 180nm DARE library. The target TID level is only 100 krad. The cells will be hardened against single event latch-up and increased leakage currents. Generating a digital standard cell library containing a complete set of functional cells is looked at. Porting of already available IP, analog or digital, is planned as well. The benefits of this new radiation hardened library are not only the reduced power consumption and higher gate density, but also the easier access to high voltage extensions and non volatile memory.

IP PORTFOLIO

More and more analog IP blocks will become available in the near future. Table 3 shows the blocks that are currently in the design stage or have been silicon proven.

Table 3 DARE analog IP blocks

IP block	Provider	Status
10b SAR ADC, 3.3V, 100 krad, slow	imec	Silicon
10b IDAC, 3.3V, 100 krad, slow	imec	Silicon
ΣΔ DAC 24b, 1.8V, 133 krad, 200 kS/s	AXIOM IC	Silicon
Linear Regulator Vin = 5V, Vout = 3.3V	CMOSIS	Silicon
Linear Regulator Vin = 5V, Vout = 1.8V	CMOSIS	Silicon
Oscillator	CMOSIS	Silicon
PLL, 1.8V, Fout = 120MHz	ICsense	Design
Bandgap, 3.3V	ICsense	Design
13b ADC, 1.8V, 100 krad, 1 MS/s	ICsense	Design
12b DAC, 1.8V, 100 krad, 50 kS/s	ICsense	Design
Linear Regulator Vin = 3.3V, Vout = 1.8V, 400 mA	ICsense	Design
Linear Regulator Vin = 3.3V, Vout = 1.8V, 30mA	ICsense	Design
15b ADC, 1.8V, 300 krad, 10 MHz	Arquimea	Design
15b DAC, 1.8V, 300 krad, 10 MHz	Arquimea	Design

SOC DESIGN: DIGITAL PROGRAMMABLE CONTROLLER

The SOC currently under design is a digital programmable controller (DPC) for Thales Alenia Space ETCA. The block diagram is shown in Figure 2. The DPC consists of 4 cores, each dedicated to a specific task: a supervision and system management micro-controller, a regulation arithmetic sequencer, a core to accommodate various communications protocols and debugging interfaces. The DPC is a mixed-mode circuit containing the following analog blocks:

- Reference voltage generation
- Power-management block with LDO's for e.g. the digital cores
- Frequency reference system (PLL) to provide the clock to the digital part
- 4 flexible ADCs with extensive input muxing capabilities
- 3 DAC current-mode outputs

- Pulse Width Modulation (PWM) outputs
- Power-on-reset circuit and under voltage detector

The DPC can be used to implement: instrument control units, remote terminal controllers, intelligent remote sensor controllers, data bus protocol translation (gateway), digitally controlled power management for power supplies & power distribution functions, motor controllers …

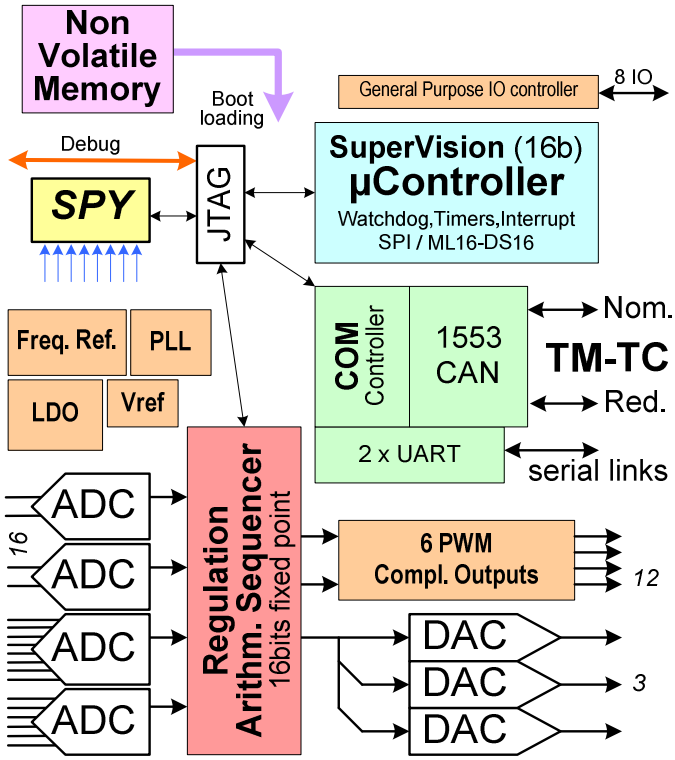

Figure 2 Block diagram of the DPC

This paper only focuses on some of the analog blocks (PLL, ADC, bandgap) and on the design methodology.

The following radiation and environmental requirements must be fulfilled:

- TID of 100krad
- SET free operation up to 60MeV.cm^2/mg for certain functionalities. The entire clock system (PLL) should be SET free in order to guarantee correct operation of the digital parts.

ADC

The SOC contains 4 ADCs that use a cyclic pipelined topology. The core of all ADCs is identical, but the amount of input muxing is different. Following functionality is foreseen for the ADCs and the input muxes:

- Up to 8 analog single-ended inputs or 4 differential inputs can be attached to a ADC core.
- The channel selection and sampling times are fully controllable by the microcontroller.
- Sensing amplifiers are foreseen to enable measurements of very low differential voltages (currents in shunt).
- The on-chip temperature sensor can also be attached to one of the ADC cores.
- Offset calibration can be done by shorting the ADC inputs.

The most important specifications of the ADC are listed in Table 4:

Table 4: ADC specifications

Specification	Value
Number of bits	13bit
Output data rate	1MS/s
Input range single-ended	0 – 2.5V
Input range differential	-1.25 - +1.25V
INL	6 LSB
DNL	1 LSB
Current consumption of 1 ADC core	6mA

Reference Voltage

The reference voltage is generated by a bandgap circuit with an external decoupling capacitance. The bandgap uses a traditional topology without analog trimming. The initial untrimmed accuracy is below 2%. The specification for the temperatures drift is +-0.6% over the entire temperature range. During design, the SET sensitivity was investigated and reduced by using large currents, additional buffer capacitances at sensitive nodes and a special startup circuit to ensure fast recovery after an SET event.

With a traditional start-up circuit, if the bandgap goes from its normal stable operating point to the 0V operating point (e.g. by a glitch on the power down input), the large external filtering capacitor will slow down the activation of the start-up circuit. In this design (Figure 3), a replica reference voltage with only a small capacitive load is used to ensure a fast reboot of the bandgap core. This fast recovery is shown in Figure 3, where a glitch of the power-down signal is simulated: the bandgap is put in power-down for 100ns. Node 'vstart' drops quickly, enabling an instantaneous reboot when the bandgap is enabled again. The effect on the actual reference voltage is minimal. Note that the bandgap itself is made insensitive to SET and as a consequence an SET of 60 MeV/mg/cm^2 on the bandgap circuit itself never triggers a reboot of the bandgap.

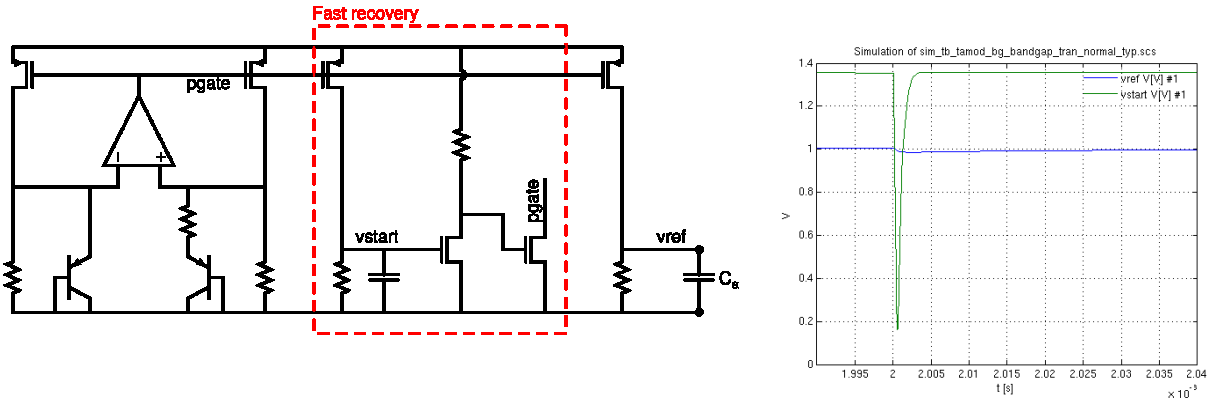

Figure 3: Bandgap reference voltage circuit and the effect of power-down glitch of 100ns on the reference voltage (blue) and vstart (green)

PLL

For a reliable operation of the digital part, it is essential that the clock generation does not produce spikes or glitches. It must also be ensured that no clock cycles are skipped to guarantee a fast response of the DC-DC regulation loops. The block diagram of the PLL is show in Figure 4 and the specifications are shown in Table 5. The complete PLL, except the capacitor of the relaxation oscillator, is integrated on-chip.

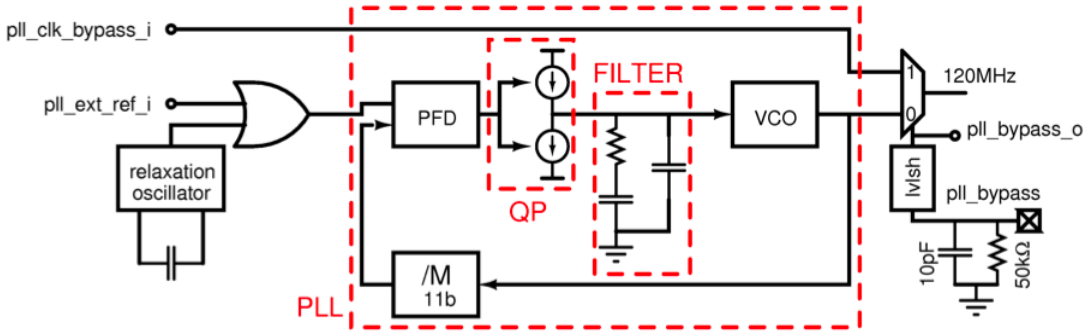

Figure 4: Block diagram of the PLL

Table 5: PLL specifications

Specification	**Value**
PLL frequency	120 MHz (± 10% after SET)
Relaxation oscillator frequency	100kHz
Cycle-to-cycle jitter over 480 cycles	14ps

The relaxation oscillator uses an external R and C to provide excellent stability and a small temperature drift. The relaxation oscillator uses triplicated comparators to achieve SET free operation. A special topology is used to achieve both low jitter and low temperature drifts; the latter is now dominated by the external components.

The Voltage Controlled Oscillator (VCO) is based on a derivative of the Maneatis delay cell [1] with sufficient high current levels and capacitor values to ensure SET free operation. The cell is less sensitive to power supply disturbances and provides lower jitter compared to a plain ring oscillator. Figure 5 shows the impact of an SET strike on an internal node of the Maneatis delay cell (most sensitive node of the VCO).

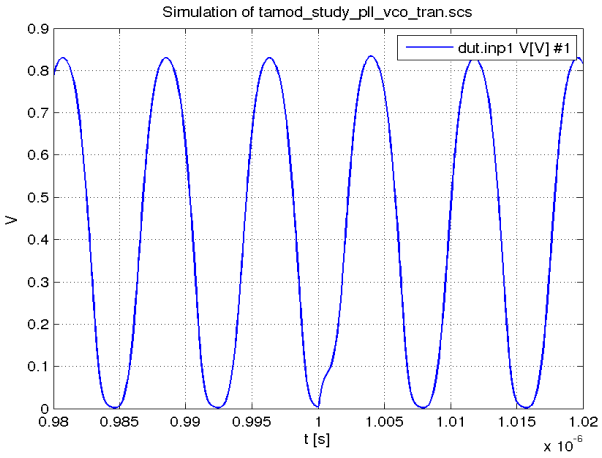

Figure 5: VCO, 60 MeV/mg/cm^2 strike at 1us

DESIGN METHODOLOGY

ICsense employs a proprietary simulation environment based on MATLAB [2]. This simulation environment drives industry standard EDA tools to perform circuit level simulation and powerful post-processing of the simulation results and automated report generation. How this design environment was further customized to enable the design of radiation hardened SOC's for space applications is explained in the next subsections.

Design for radiation

In order to make a robust design for space applications, several aspects related to SET and TID have been incorporated in the analog design flow.

SET: The effect of an SET strike is simulated by injecting a double exponential current pulse on a certain node of the circuit [3]. The total inject charge corresponding to an LET of 60MeV.cm^2/mg is 1.2pC. The design environment allows injecting this pulse in any circuit node at any wanted point in time. This system is used to accommodate following flow:

1. Inject an SET pulse in every circuit node under typical conditions. This produces a shortlist of sensitive nodes.
2. Perform SET simulation for all these sensitive nodes over PVT corners. An iterative procedure is carried out to adapt the nodes if the specifications are not achieved due to the SET strike by adapting the current levels, adding buffer capacitances or performing topology changes to reduce the sensitivity of a specific node.
3. Final verification by injecting all nodes again in some of the worst-case corners for SET sensitivity.

For DC-type circuits like bandgaps, the moment of the SET strike is not relevant. However, this is not the case for oscillators. For these blocks, the simulations are very time-consuming since the time at which the SET strikes relative to the clock period is important. This procedure is used during block-level design to ensure good performance under SET strikes. On top-level simulations, this is used to ensure that an SET event on e.g. the bandgap does not impact the PLL output.

TID: To make the circuit robust for TID, a combination of various techniques are used:

- TID will result in Vth shifts of the devices, thus reducing the margins on the operating points of the transistors. The worst-case Vds-Vdssat across all PVT combination is monitored for all devices and this allows the designer to quantify the margins of each device and optimize the operating point for robustness across corners.
- The induced Vth shifts due to TID will depend on the bias conditions of the devices. Special care is taken to ensure identical operating points of all devices belonging to one matching structure under all operating modes. This ensures that, even when blocks are powered down, all matching structures are identically biased.
- TID can generate leakage paths between N+ regions at different potentials. The DARE ADK provides an additional DRC rule check to flag N+ regions at different potentials that are not interrupted by P+ regions
- The analog blocks with highest matching sensitivities are put on 1.8V supply domain with thin-oxide devices to minimize TID sensitivity.
- For critical devices on the 3.3V domain, the enclosed layout transistors (ELT) from the DARE ADK are used.

Wreal Modeling

When building a complex SOC, it is of utmost important to guarantee that all functional operation modes are verified to minimize the risk and to make a first-time right design realistic. A proven approach is to use top-down bottom-up design strategy. This approach consists of generating high-level models of each block to verify the functionality right from the start of the project.

The models used in the project employ Verilog-AMS with wreal data types [4] for the analog parts. Wreal is a dedicated data-type that is continuous in amplitude, but discrete in time. These properties ensure that it can be simulated by a standard digital simulator in an event-based fashion. Care is taken during the writing of the models that no analog parts of the Verilog-AMS language are used. This approach ensures that the generated models can be simulated in a plain digital simulator at a very high simulation speed.

Another advantage of this approach is that the analog and mixed-mode simulations can employ the same set of identical models, eliminating the risk of the analog and digital team having different representations of the same blocks. The wreal models are also used to perform top-level mixed-mode simulations where certain analog parts of the chip use full transistor level accuracy, while other analog blocks use the wreal model and the digital part is simulated in Verilog. This approach ensures that good trade-offs between simulation accuracy, coverage and simulation speed can be obtained in complex mixed-mode designs.

CONCLUSION

The DARE library has evolved from a purely digital standard cell offering to a mixed-signal capable technology platform. In the near future more analog IP blocks will become available through ESA funded activities. Once the DTV radiation results become available a better modeling of the analog transistor behavior will be included in the ADK. Porting to a XFAB 0.18 technology with mixed-signal and high-voltage options is foreseen in the near future. The design of a complex SOC for space applications shows that highly reliable analog blocks are being developed. A dedicated under-radiation simulation methodology is needed to analyze, improve and characterize the SEE performance of these blocks.

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