RADIATION HARDENED MIXED-SIGNAL IP WITH DARE TECHNOLOGY

icsense

ThalesAlenia Space
A Thales / Finmeccanica Company

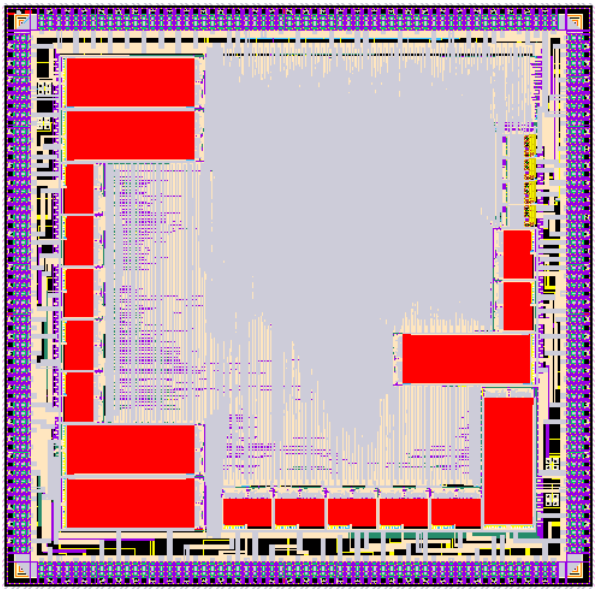
imec

OUTLINE

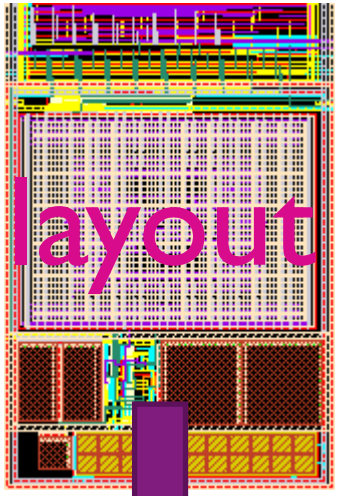
- Introduction
- DARE+ activity
- DARE legacy
- Analog IP portfolio
- DARE technology porting
- SOC design
- Analog rad-hard design methodology

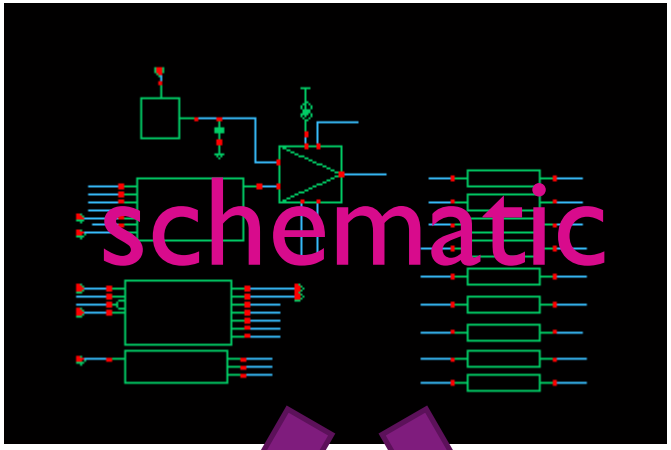
AMICSA 2010: KNUT ASIC

- First DARE Mixed-Signal Flight Models
- TESAT Spacecom GmbH & Co.KG
- UMC 180nm 1P6M + MiM
- Mixed Signal ASIC
  - 88 mm^2
  - 120 I/O
  - ADCs and DACs
  - ELT and Guardrings
- Digital-on-Top integration



AMICSA 2010: INTEGRATION OF ANALOG BLOCKS

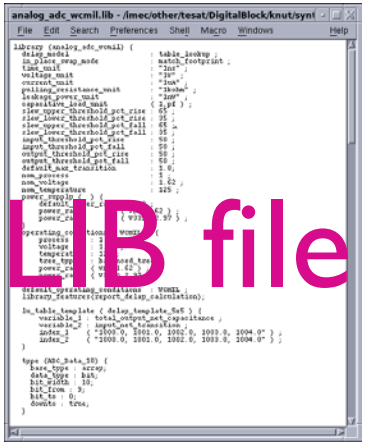


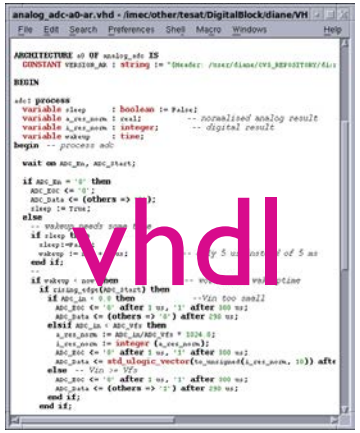


abstract generator
LEF script

analog simulation
LIB template

model description

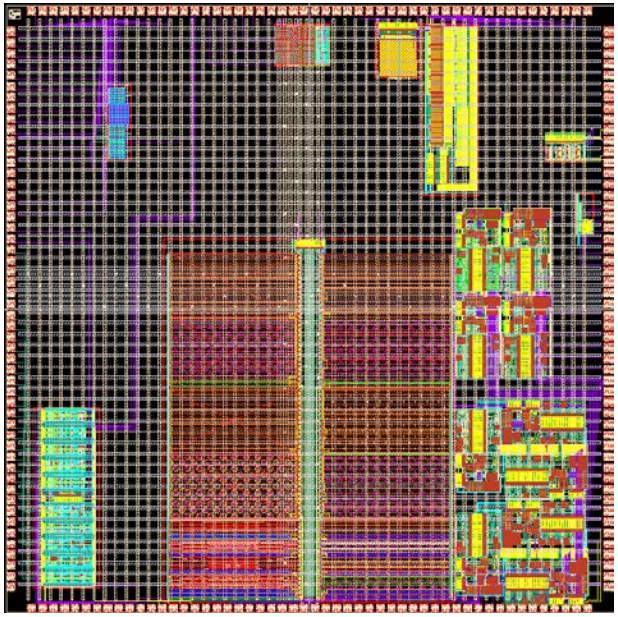




DARE+ ACTIVITY

- ESA contract 40000104087/11/NL/AF
- Kick-Off: 1 June 2011
- End Date: 1 June 2013
- Objective: *"Provide a mixed-signal capable microelectronic technology for platform and payload elements for spacecrafts on Jovian missions"*
  - Improve existing & create new library elements (for use in Mixed-Signal ASICs)
  - (Mixed-Signal) Demonstrator
- 3 test vehicles:
  - Devices Test Vehicle (DTV) — Taped out Jan 2012
  - Library Test Vehicle (LTV) — Tape-out Oct 2012
  - Application ASIC (XentiumDare) — Tape-out Oct 2012

DEVICES TEST VEHICLE (1)



- Test vehicle for TID testing of analog devices in the UMC L180 technology with mixed-signal processing option
- Improve ELT transistor model for analog design
- Create Analog Design Kit (ADK)
  - Dedicated symbol for schematics
  - Dedicated pcell for layout
  - Dedicated rule decks for physical verification
- Ringoscillators and Cascoded current mirrors added for model verification

DEVICES TEST VEHICLE (2)

- MOS transistors
  - 1.8V / 3.3V
  - RVT, Low-VT
  - Triple
  - ELT / straight

(Leakage currents VT-shift, noise, matching, mobility, breakdown voltage)

- Bipolar
  - 2 sizes
  - 3 layout flavors

(Beta, noise, leakage current, mismatch, transit time)

- Diodes
  - All same area
  - Different aspect ratios

(Reverse current, ideality factor, barrier potential)

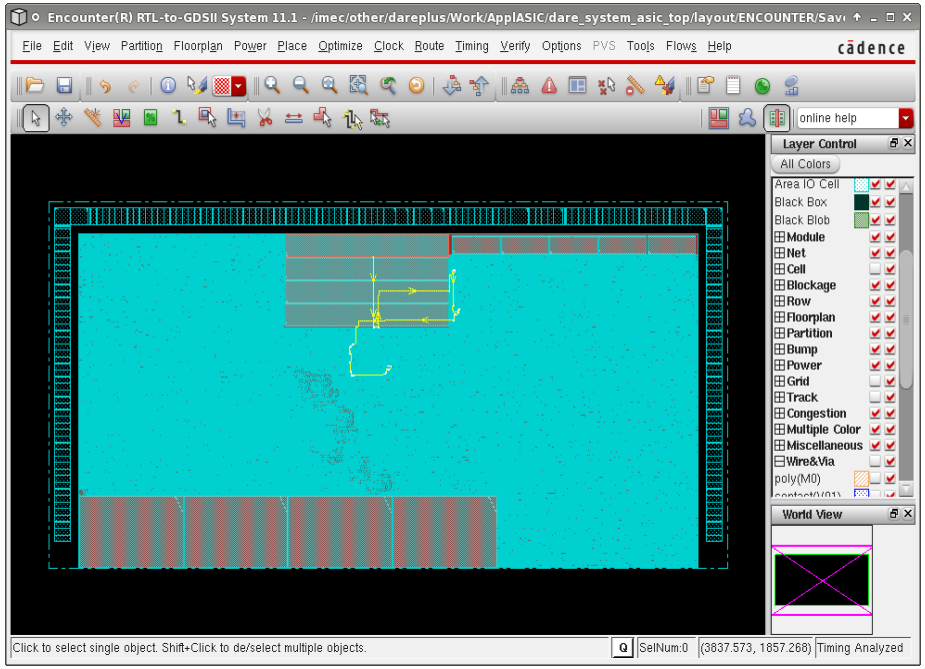
First IV-measurements up to 100 krad on MOS transistors have been done very recently.

LIBRARY TEST VEHICLE (1)

- Test vehicle for TID and SEE testing of library improvements and additions in the UMC L180 mixed-signal technology
- Improvements:
  - Single Port SRAM compiler
  - Phase Locked Loop (SEE hardening)
  - LVDS with Extended Common Mode Range (-4V to +5V)
  - Slew Rate Control (reducing # PG pads)
- Additions:
  - Dual Port SRAM compiler
  - Linear Voltage Regulator (from 3.3V to 1.8V)
  - Voltage Reference (Vref=1.25V)
  - Integrated Clock Gating cells

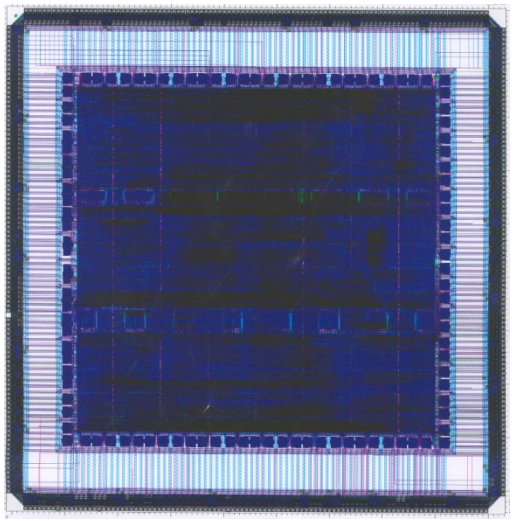
APPLICATION ASIC

- XentiumDare
  - Recore Systems (Enschede, NL)
  - Xentium VLIW DSP core
  - Memory Tile, Network-On-Chip, EDAC, SpW interfaces, ADC interface, DAC interface, UART, GPIO, ...
  - 5mm x 10mm
- Single Event tests scheduled Q1 2013
- No TID tests
- Unfortunately ADC and DAC not yet integrated.



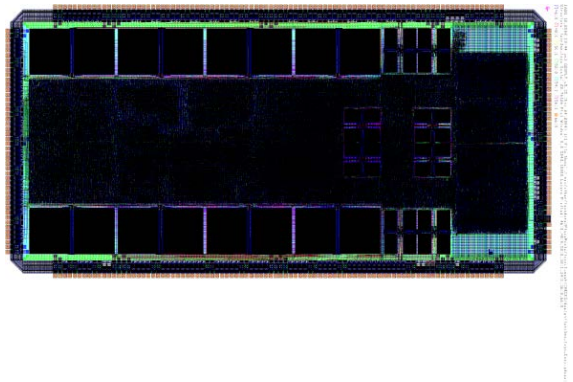
DARE ASICS: ESA PROJECTS

DROM

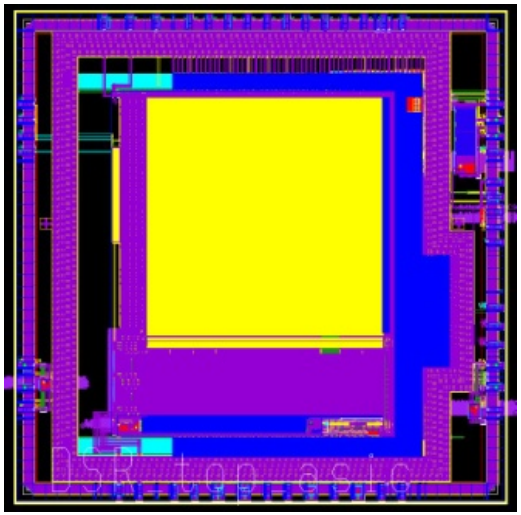


First functional DARE silicon

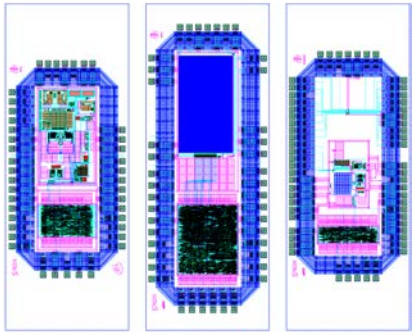
LEONDARE

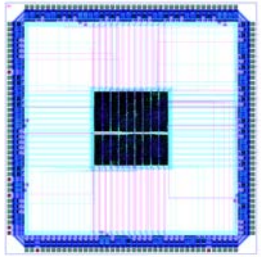


SSOC



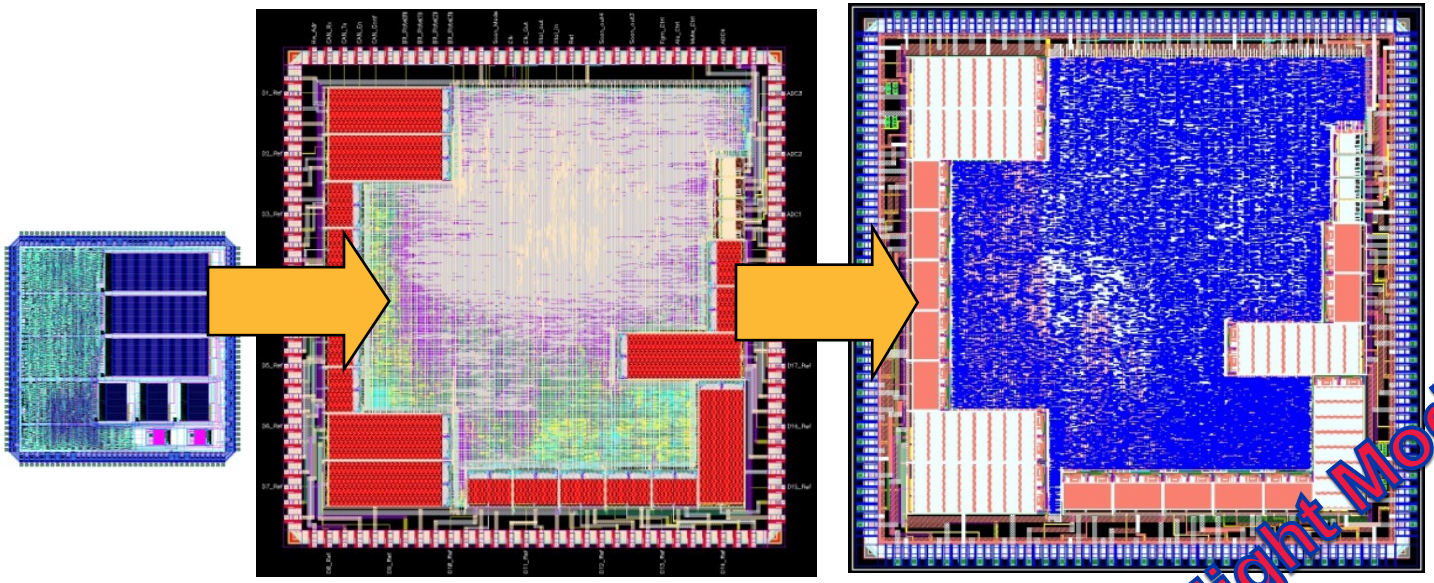
CIS Port





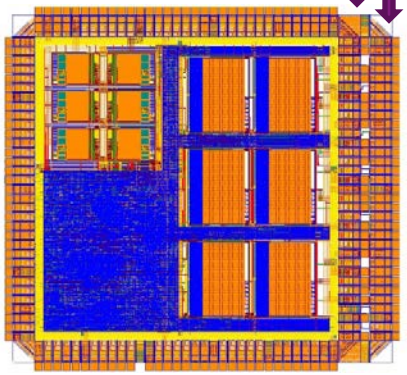
Muller-C gate added

DARE ASICS: CUSTOMER CHIPS

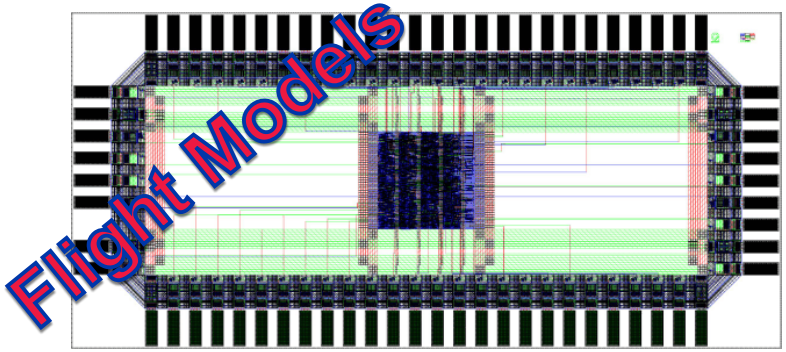


Flight Models

Dual bond



(Slow)
ADC & DAC
IP blocks



Flight Models

DARE ANALOG IP (I)

IP block	Provider	Status
10b SAR ADC, 3.3V, 100 krad, slow	imec	Silicon
10b IDAC, 3.3V, 100 krad, slow	imec	Silicon
Bandgap, 1.8V	imec	Design
PLL, 1.8V, Fin > 10 MHz	imec	Design
Linear Regulator, Vin = 3.3V, Vout = 1.8V, 50mA	imec	Design
ΣΔ DAC 24b, 1.8V, 133 krad, 200 kS/s	AXIOM IC	Silicon
Linear Regulator Vin = 5V, Vout = 3.3V	CMOSIS	Silicon
Linear Regulator Vin = 5V, Vout = 1.8V	CMOSIS	Silicon
Oscillator	CMOSIS	Silicon
PLL, 1.8V, Fout = 120MHz	ICsense	Design
Bandgap, 3.3V	ICsense	Design
13b ADC, 1.8V, 100 krad, 1 MS/s	ICsense	Design
12b DAC, 1.8V, 100 krad, 50 kS/s	ICsense	Design
Linear Regulator Vin = 3.3V, Vout = 1.8V, 400 mA	ICsense	Design
Linear Regulator Vin = 3.3V, Vout = 1.8V, 30mA	ICsense	Design

DARE ANALOG IP (2)

IP block	Provider	Status
12b/10b ADC, 1.8V, 300 krad, 10/100 MHz	Arquimea	Design
12b/10b DAC, 1.8V, 300 krad, 10/100 MHz	Arquimea	Design
19b/16b/14b ADC, 1.8V, 0.1/1.0/10 MHz	Arquimea	Design
19b/16b/14b DAC, 1.8V, 0.1/1.0/10 MHz	Arquimea	Design
LNA	Arquimea	Design
Charge Amplifier	Arquimea	Design
Voltage Reference	Arquimea	Design
4-channel Analog Multiplexer	Arquimea	Design
Gaussian Shaper	Arquimea	Design
Power Amplifier	Arquimea	Design

DARE TECHNOLOGY PORTING

- XFAB 0.18
- Initial focus is on
  - digital standard cell libraries
  - Dual Port SRAM
- TID target = 100 krad
- SEU hardened FF, SEL & SET mitigation
- Availability of NVM (SEL monitoring)
- Availability of HV

QUESTIONS ?

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