

ADVANCES IN RADIATION HARDENED MIXED-SIGNAL TECHNOLOGY

D. Kerwin, A. Zanchi, A. Wilson, K. Merkel, J. Colley
Aeroflex Colorado Springs, Inc.
4350 Centennial Blvd.
Colorado Springs, Colorado 80919
USA

david.kerwin@aeroflex.com

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- ▼ **Introduction**
- ▼ **Case Study 1: Smart Sensor SoC ASIC**
- ▼ **Case Study 2: 16-bit Pipeline ADC**
- ▼ **Case Study 3: 4-Channel Voltage Supervisor**
- ▼ **Summary**

Aeroflex Radiation Hardened Mixed-Signal ASICs



▼ Aeroflex

- **Supplier of radiation hardened digital ASICs since 1985, and radiation hardened mixed-signal ASICs since 2000**
- **Serving Space/Satellite, Medical, Security, and Industrial Markets**
- **QML-V Approved Quality Management System**
- **Over 700 space qualified ASICs since 1980**

▼ Aeroflex uses high volume commercial foundries

- **QML-V Approved Foundry Partners**
- **Active SPC programs**

▼ Aeroflex Radiation Hardened Technology

- **Commercial RadHard Technology Libraries**
- **One-Time Electrically Programmable Metal Fuse module**

▼ Supply Chain:

- Nine foundry partners world-wide (US, Europe, Asia)
 - ▼ Five QML-V foundry partners (US & Asia)
- Aeroflex Assembly, Test, Qualification
- In-House Reliability & FA Labs

▼ Strong Mixed-Signal Design Team

- 32 Mixed-Signal Designers, each with minimum 15 years experience in Radiation Hardened ASIC design

▼ Key Success Factors

- Transistor Modeling in house
- Qsim & SETsim for SET modeling
- Reliability Analysis & Modeling: Aeroflex Reliability Design Rules and Safe Operating Area Simulations (Hot Carrier Models, Electromigration & TDDDB Rules)

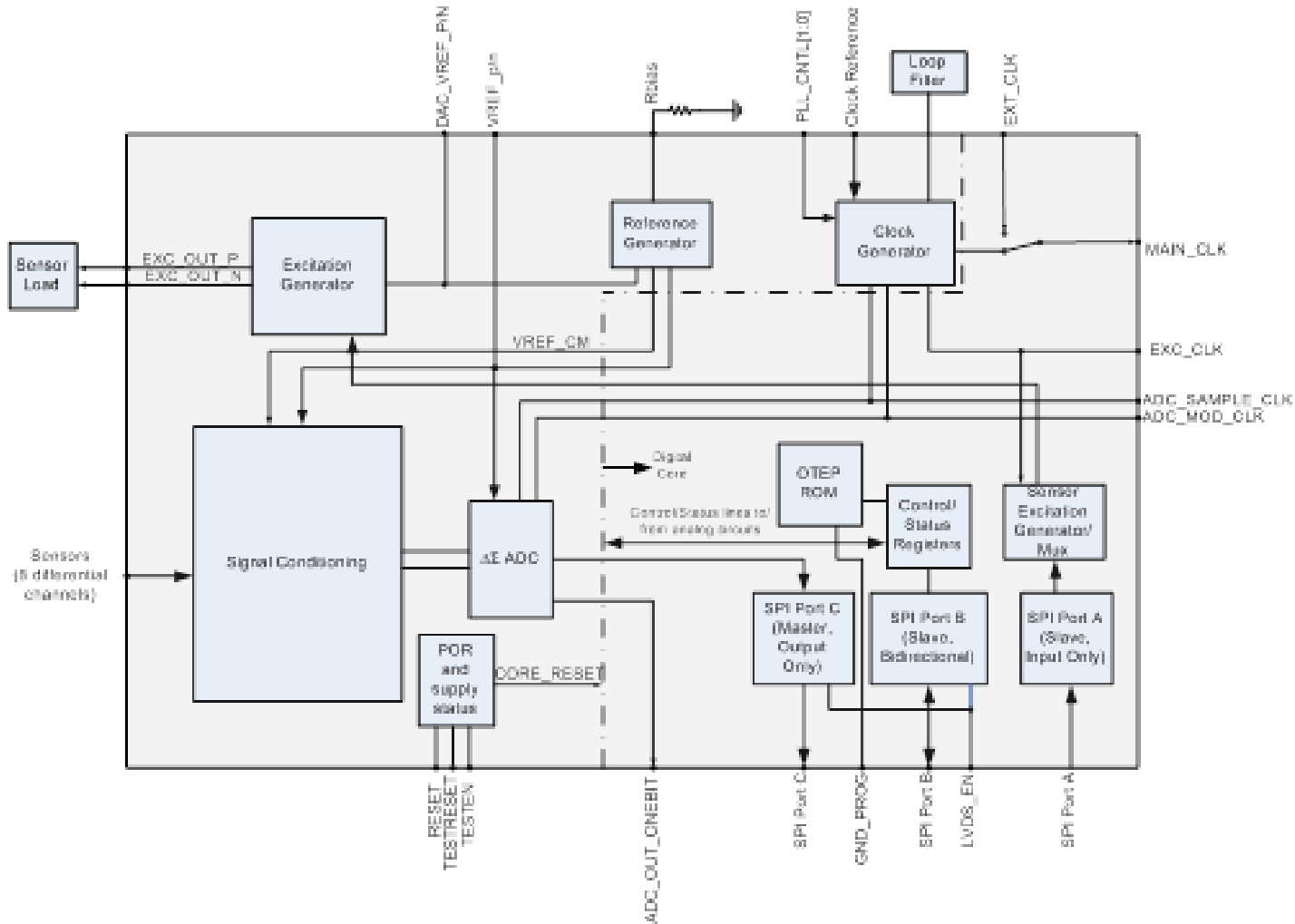
▼ Radiation Testing:

- Aeroflex Radiation Test facilities for Gamma & X-Ray TID, Low Dose-Rate TID, 14 MeV Neutrons, Flash X-Ray, Laser for SET
- Partner Facilities for Heavy Ion, Proton, Thermal Neutron/Nuclear Reactor testing, pico-second Single and Dual Photon Absorption Laser Testing, High Dose Rate e-beam and flash X-Ray

▼ Radiation Hardened Analog & Digital IP:

- Digital Libraries, I/O's and Extensive Library of Analog IP Blocks focused on high-precision, base-band signal conditioning, data conversion, and actuation

Case Study 1: UT08SC14ADV045 Smart Sensor ASSP



▼ Complete Instrumentation System:

- Includes circuitry to excite and precisely measure the response from 11 sensor types.
- Supported Sensors:
 - ▼ Resistance Thermometer, Thermocouple, LVDT, Strain Gauge/Load Cell, Inductive and Transformer-based Position, Absolute and Relative Pressure Sensors, Hall Effect probe, Photodiode, Accelerometer, Tachometer, and other types of Sensors.
- Excitation generator includes a 14-bit DAC with a high current, high-voltage differential output.
- Eight high-voltage differential signal inputs are provided, with configurable signal conditioning.
- 14-bit 45 kSps delta-sigma analog-to-digital converter (ADC)

▼ Complete Instrumentation System:

– Data I/O:

- ▼ Digital data word transmitted through a Low-Voltage Differential Signaling, Serial Peripheral Interface (LVDS SPI) port.
- ▼ A second LVDS SPI port is used for configuration, control, parameter trim, and access to internal registers

– Clock Generation:

- ▼ A clock generator block generates the necessary internal clocks from a low-frequency reference.

– Voltage Regulators:

- ▼ Internal regulators derive necessary supply voltages and references from +/-6V and +3.3V power supply inputs.

UT08SC14ADV045 Smart Sensor ASSP

▼ Complete Instrumentation System:

– NVM:

- ▼ Aeroflex Radiation Hardened One-Time Electrically Programmable Read-Only Memory (RH OTEP ROM) provides storage for reference trim data, configuration data, and user configurable program storage.

– Applications:

- ▼ Nuclear Power Instrumentation Monitoring
- ▼ Spacecraft Telemetry
- ▼ Radiation Oncology Equipment Motor/Motion Control
- ▼ Nuclear Waste Monitoring

UT08SC14ADV045: Key Performance Parameters:

| | |
|---|---|
| Excitation Output | 14-bit DAC with differential voltage-mode output up to 20Vp-p, up to 140mA. Sine/square/triangle or arbitrary function outputs. |
| Sensor Inputs | 8 multiplexed differential high-impedance user inputs; input range -5V<V _{in} <+5V |
| Signal Channel | Programmable gain range 0.18 to 100, 15 kHz bandwidth, includes anti-alias filter |
| A/D Converter | 14-bit, 3 rd -order delta-sigma, 45kSps |
| Typical channel mismatch | 0.04% to 100°C, 0.07% to 200°C |
| Typical absolute measurement error | 1% to 100°C, 4% to 200°C |

0.35 μm BCD Technology



| | |
|---------------------------------|---|
| Technology Type | 0.35 μm BCD (Bipolar-CMOS-DMOS) |
| Minimum Feature Size | 0.35 μm |
| Well Structure | Triple-Well (Substrate Isolated) |
| Transistors Used | 3V Enhancement Mode NMOS & PMOS (self-aligned) 8V Enhancement Mode NMOS & PMOS (self-aligned) 12V Enhancement Mode Drain-Extended NMOS & PMOS 20V PNP BJT (vertical) |
| Metallization and Interconnects | 4LM, Tungsten Plugs, CMP Planarization |
| Resistors | Diffusion Resistors, Poly Resistors (non-salicided), Hi-Poly Resistors |
| Capacitors | PiP, MiM, MOS-caps |
| Aeroflex Enhancements | Aeroflex RH OTEP Metal Fuse |

**Wafer Foundry QML-V approved as a supplier to
Aeroflex**

**Aeroflex RH Digital Library, I/O's, and Analog IP
Blocks**

UT08SC14ADV045 Radiation Requirements



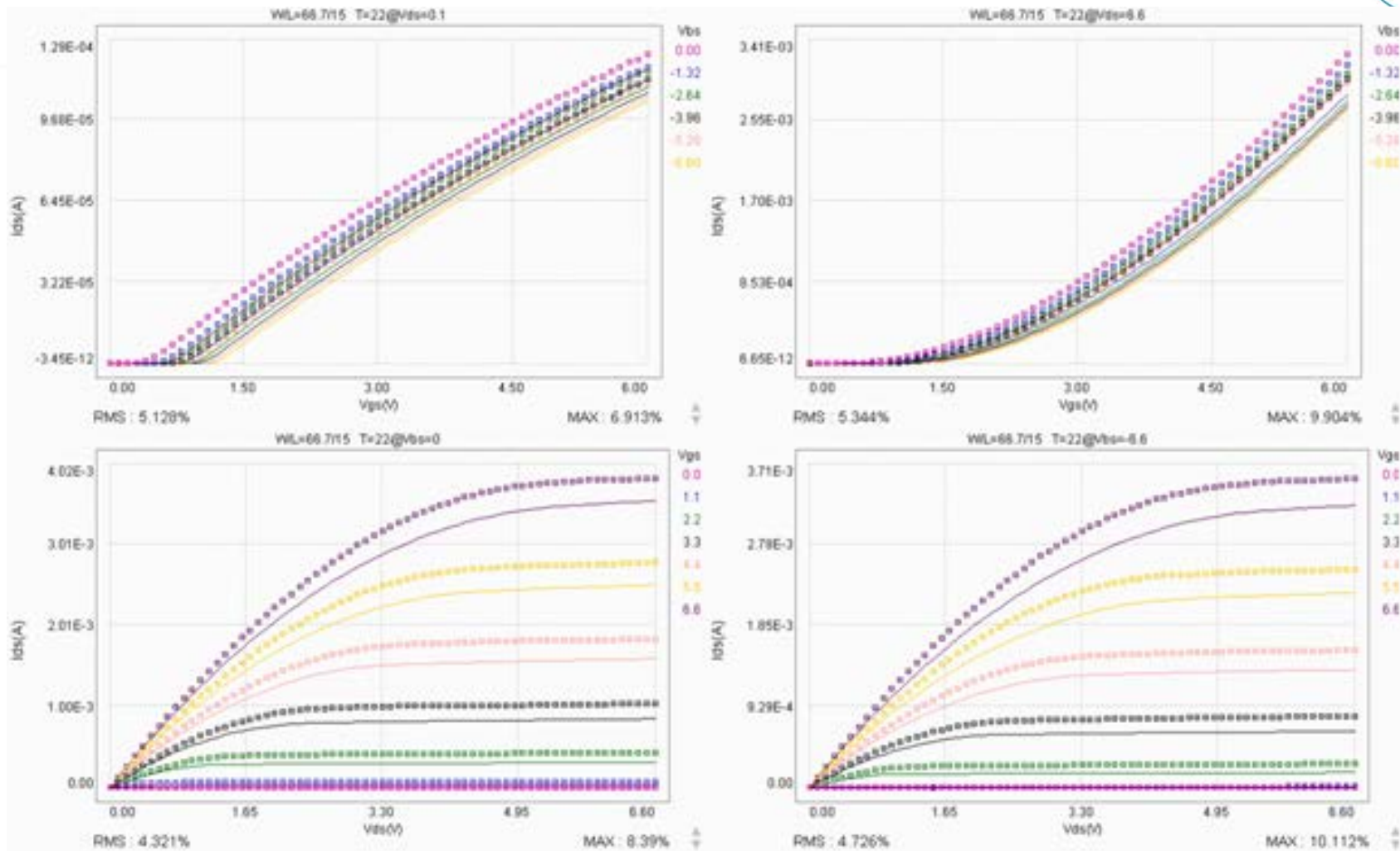
| Environment | Requirement |
|-------------------------------------|---|
| Gamma Ray Total Ionizing Dose (TID) | 100krad(Si) at a dose rate of 2.8mrad(Si)/sec |
| Neutron Induced Upset (NIU) | < 1E-11 errors/bit/day |
| Neutron Induced Latch-Up (NIL) | Immune (5E11 neutrons/cm ² , peak energy < 2MeV) |
| Temperature | 200°C max. operating |

Challenges:

Transistor characteristics change with total ionizing dose.

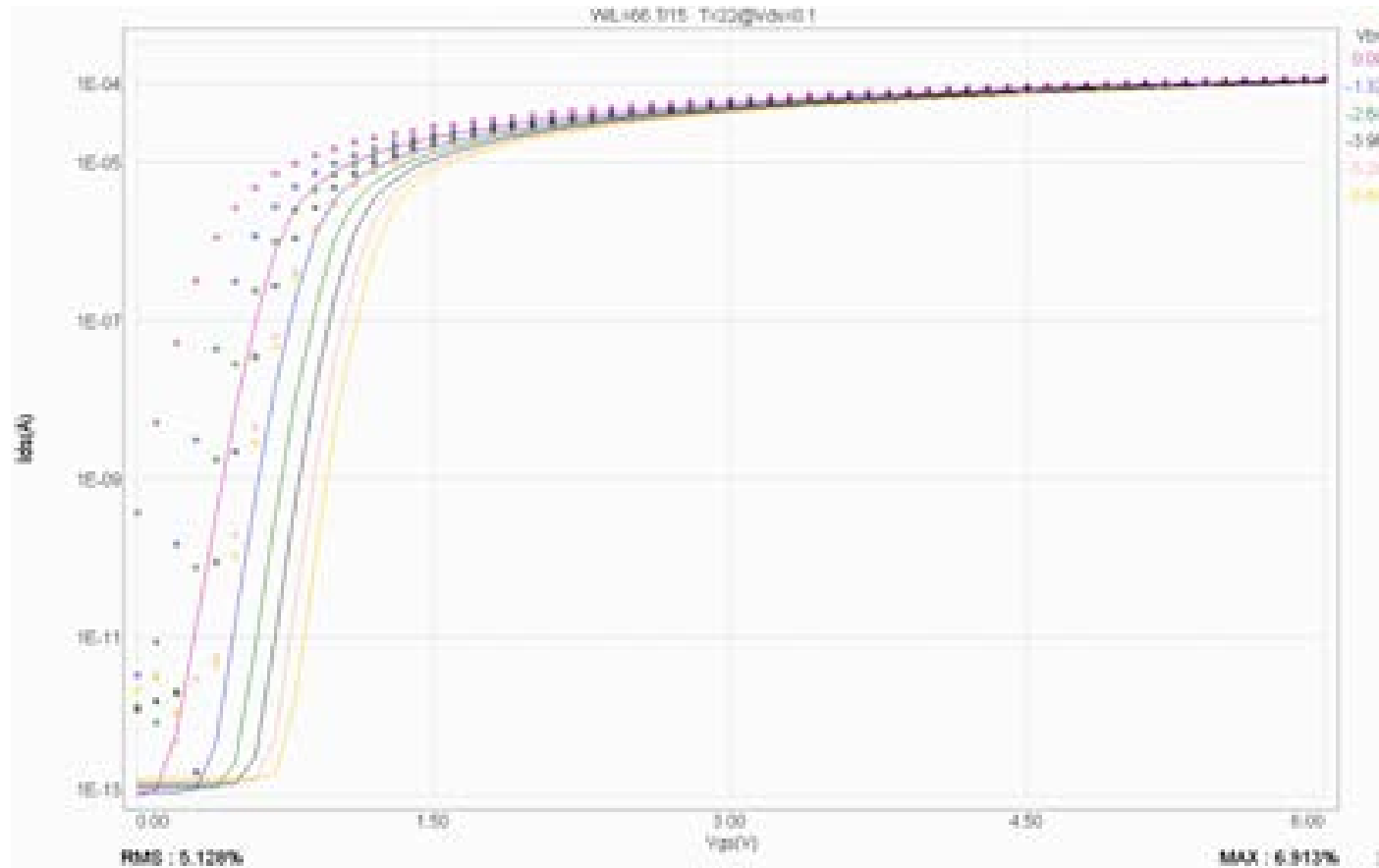
BSIM 3v3 models from foundry inadequate to model post-radiation performance.

Foundry Models compared to 100krad(Si) Data



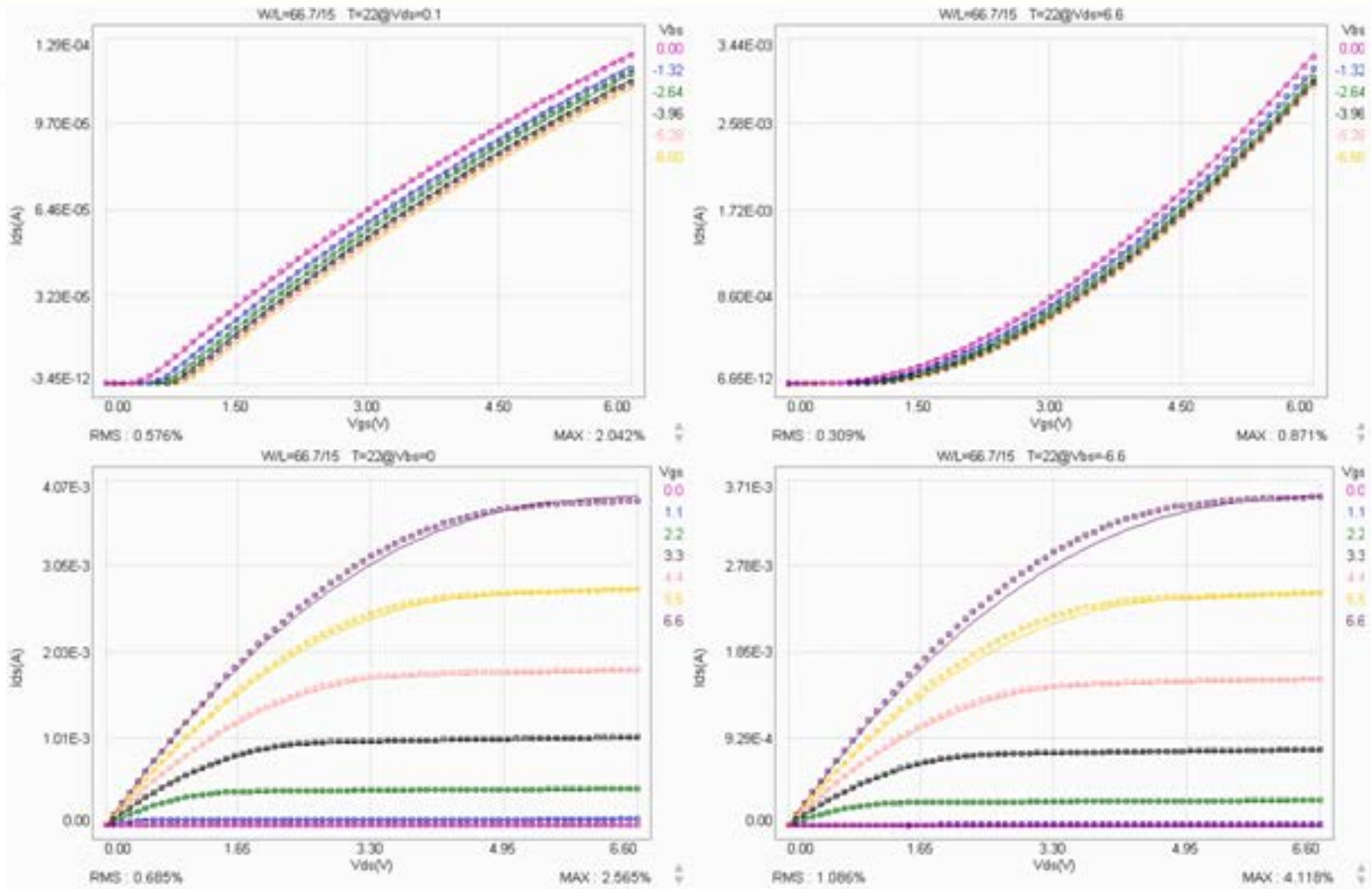
Poor Foundry Model Fit to Data after 100krad(Si)

Foundry Models compared to 100krad(Si) Data



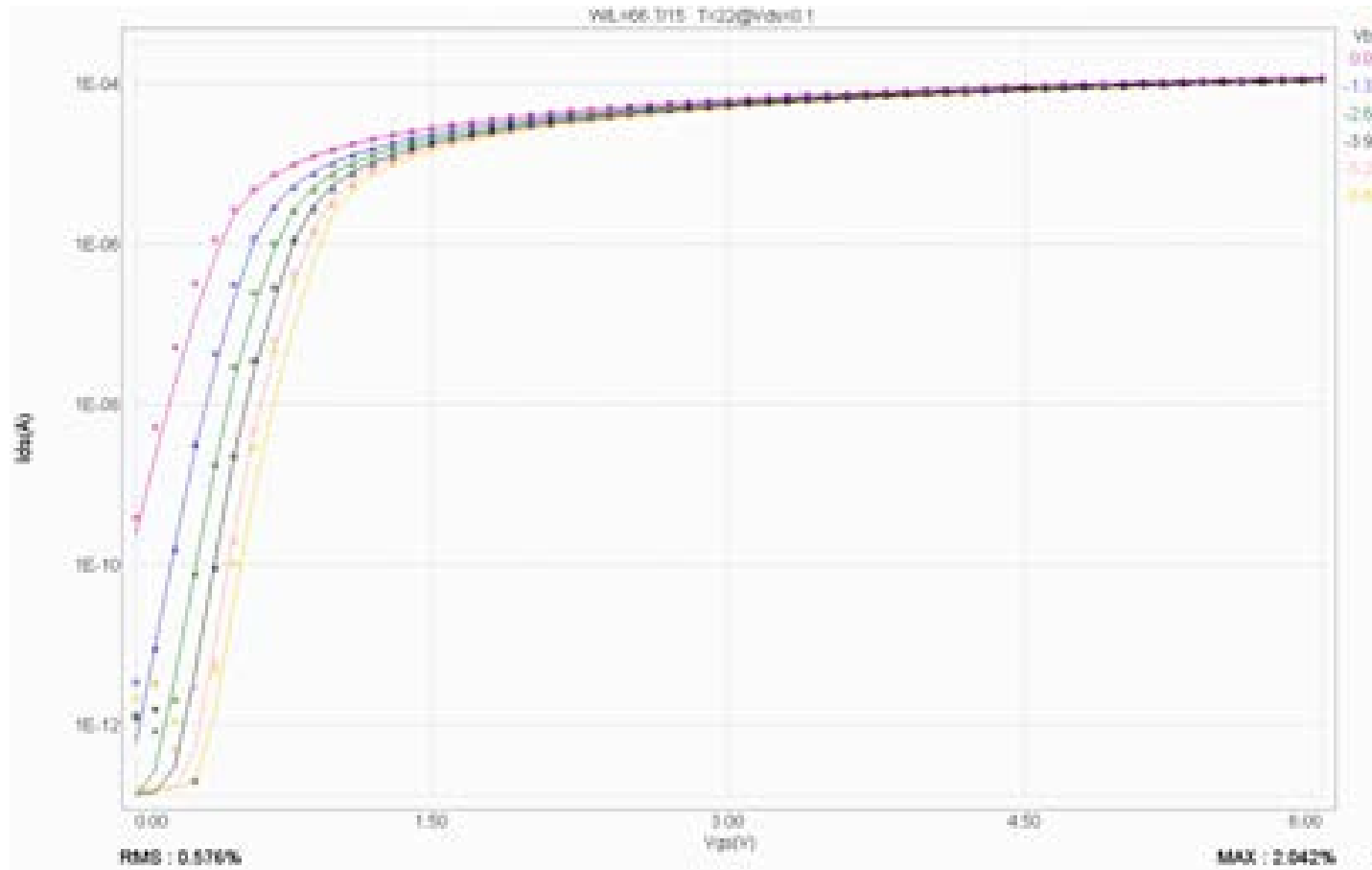
Poor Foundry Model Fit to Data after 100krad(Si)

Aeroflex Models compared to 100krad(Si) Data



Aeroflex Models Fit the 100krad(Si) Data well.

Aeroflex Models compared to 100krad(Si) Data



Aeroflex Models Fit the 100krad(Si) Data well.

UT08SC14ADV045 First Pass Silicon Results

| Test | Results |
|---------------------------|--|
| Total Ionizing Dose (TID) | PASSED 100krad(Si) at 200rad/sec |
| Low-Dose Rate TID | PASSED 100krad(Si) at 10mrads(Si)/sec |
| NIU | NO UPSETS after $6.8E11$ n/cm ² |
| NIL | NO LATCH-UP after $6.8E11$ n/cm ² |

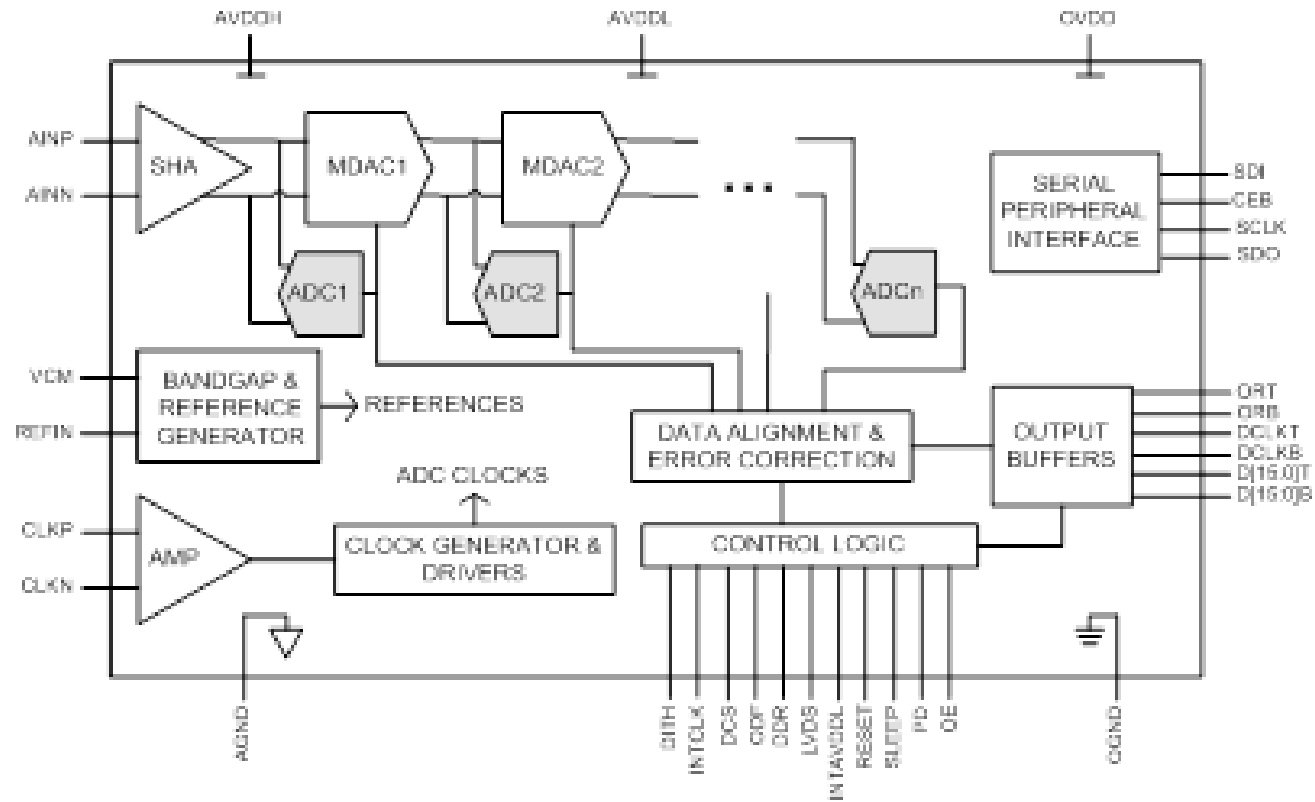
Successful 1st Pass Silicon due to Aeroflex developing its own compact transistor models using transistor test structures on its Technology Characterization Vehicle

Case Study 2: 16-bit Pipeline ADC

▼ Ideal for Telecommunication and Imaging applications:

- 16-bit, 40-MSps CMOS pipeline ADC
- Excellent noise (76dBFS SNR) and distortion (95dBc SFDR)
- 2.5Vp-p input
- Sample-and-Hold Amplifier (SHA)
- Duty-Cycle Stabilization produces 50% clock phases even with 20% - 80% duty cycle skew in external clock
- Internal dither function for improved linearity of the conversion of small signal analog inputs
- Linearity: $\pm 2.5\text{LSB}$ INL and $\pm 0.25\text{LSB}$ DNL.
- Two output data formats: straight binary and 2's complement

UT16AD80P, UT16AD40P, UT14AD20P



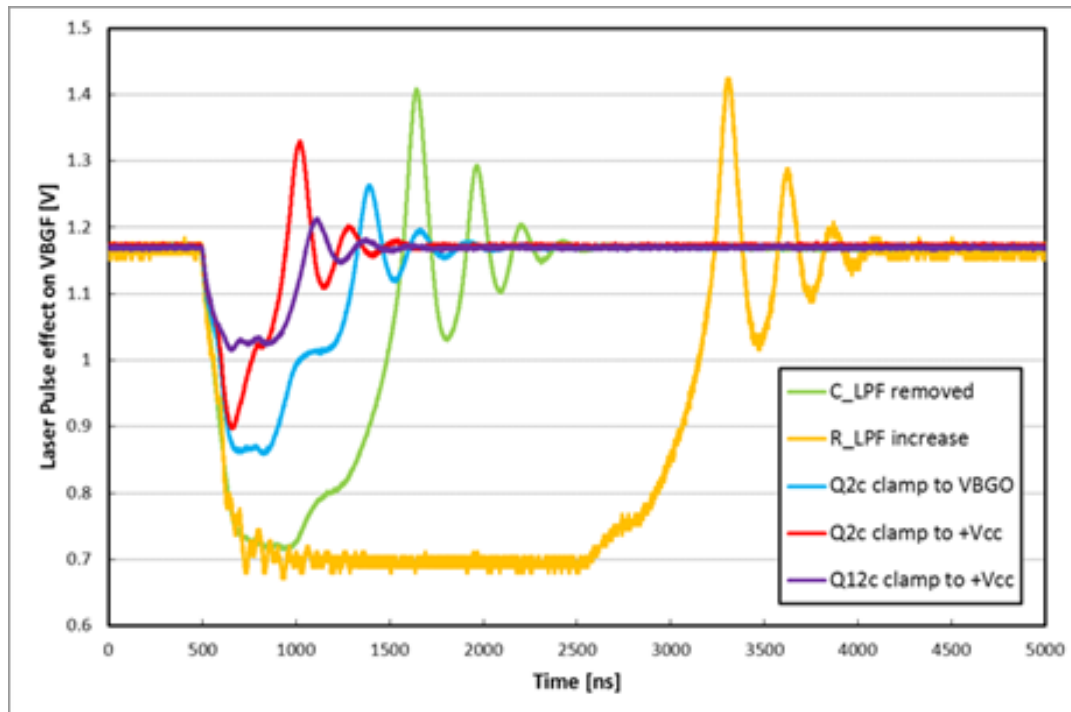
0.18 μ m Triple-Well 6LM Mixed-Signal CMOS

Table VI: Key Technology Features for UT16AD40P

| | |
|---------------------------------|--|
| Technology Type | 0.18 μ m Mixed-Signal CMOS |
| Minimum Feature Size | 0.18 μ m |
| Well Structure | Triple-Well (Substrate Isolated) |
| Transistors Used | 1.8V Enhancement Mode Isolated NMOS & PMOS (self-aligned) 1.8V Enhancement Mode non-isolated NMOS (self-aligned) 3.3V Enhancement Mode Isolated NMOS & PMOS (self-aligned) 3.3V Enhancement Mode non-Isolated NMOS (self-aligned) Native non-isolated NMOS Bipolar NPN (vertical) |
| Metallization and Interconnects | 6LM, Tungsten Plugs, CMP Planarization |
| Resistors | Diffusion Resistors, Poly Resistors (non-salicided), Hi-Poly Resistors |
| Capacitors | MiM, MOS-caps |
| Aeroflex Enhancements | P-type varactors, Low Dielectric Absorption MiM Capacitors, RH OTEP Metal Fuse |

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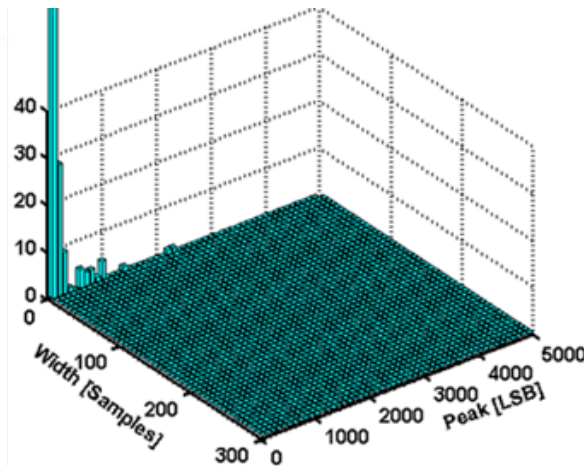
UT16AD40P Design Challenges



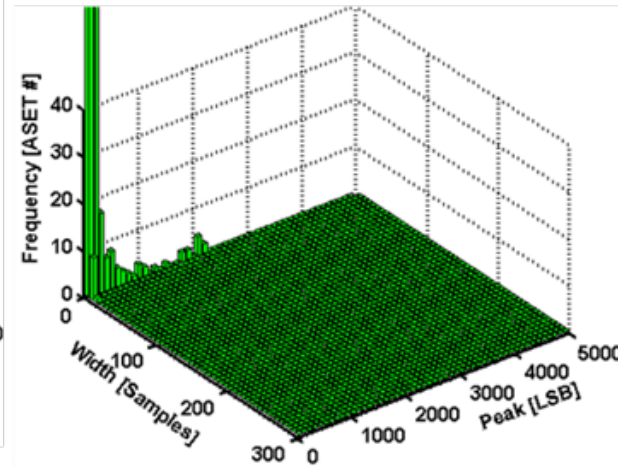
Laser testing of Bandgap on TCV showed Long Duration SET Pulse (LDP – yellow line >).

Subsequent TCV modifications with clamps to V_{BGO} or V_{CC} gave the needed improvement (purple line, < 500nsec) before tape-out.

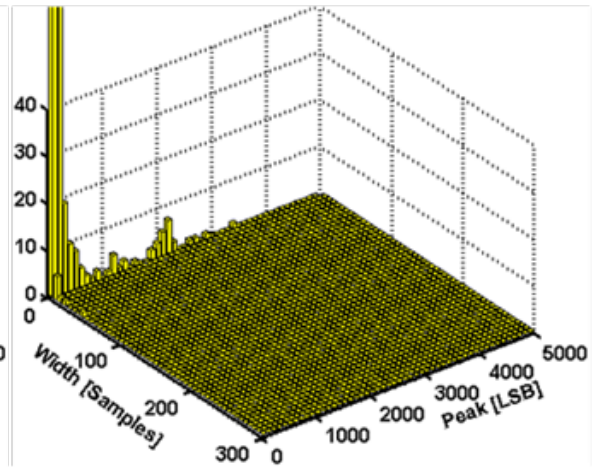
3D Methodology for Rating SET



(a) LET = 30 MeV-cm²/mg



(b) LET = 60 MeV-cm²/mg

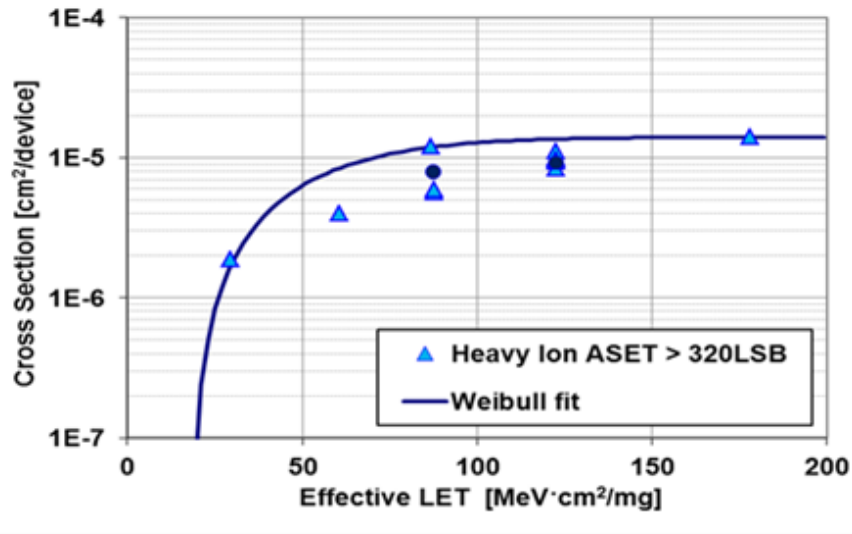


(c) LET = 87 MeV-cm²/mg

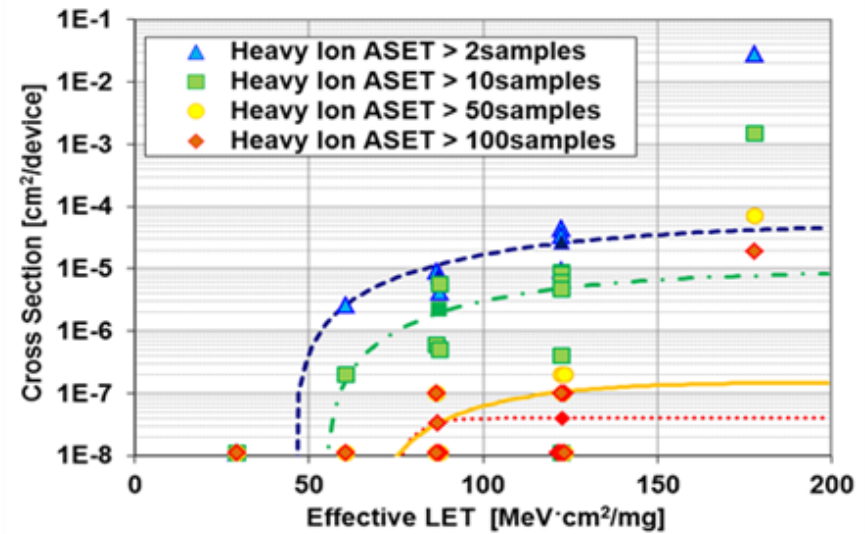
Aeroflex using 3D SET Rating Methodology for providing the user detailed information about SET performance of its ADC's

User can see both duration and extent (e.g. in LSB peak of ASET) as a function of LET as shown above.

Generation of 2D Cross Section Curves



(a)



(b)

Generation of traditional 2D Cross Section Curves is easily accomplished by integrating 3D histograms over desired duration and/or extents

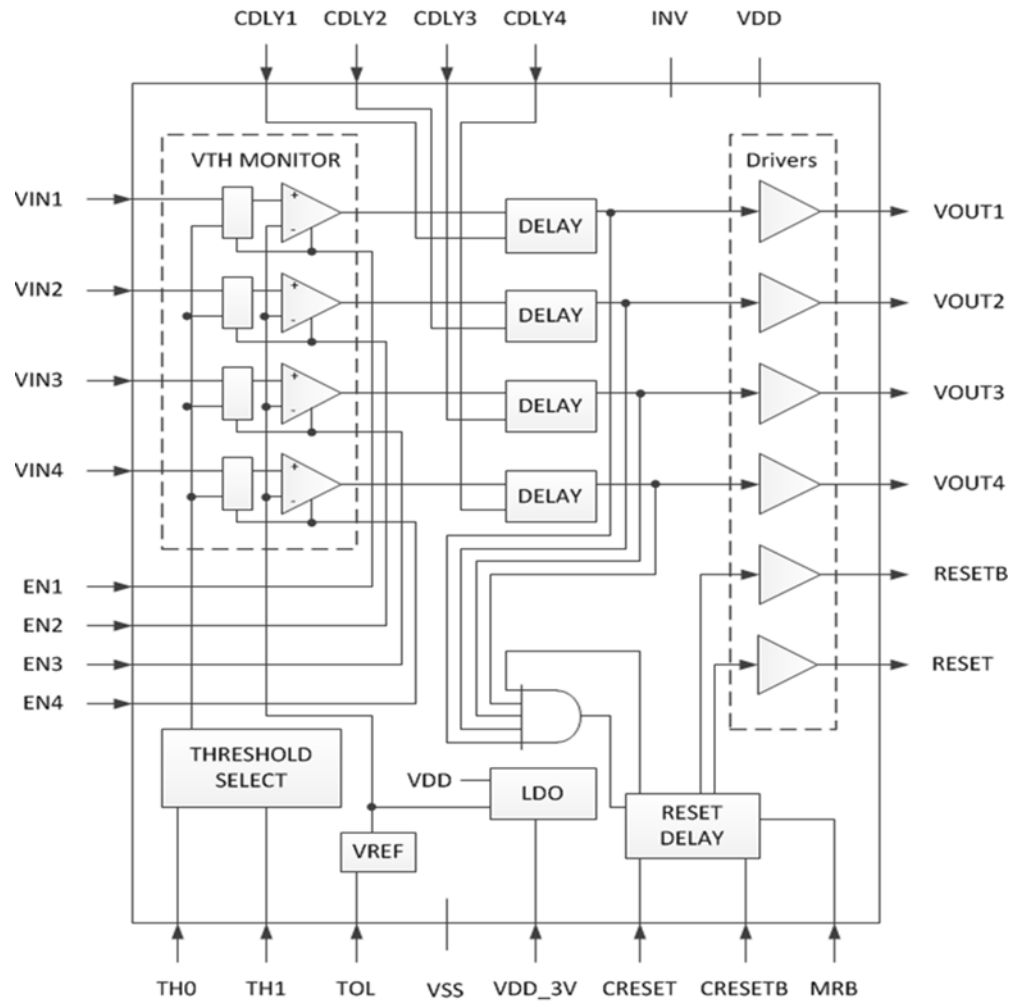
- (a) Cross Section for extents > 320 LSB's (regardless of duration)**
- (b) Cross Section for durations of 2, 10, 50, 100 sample clocks (regardless of extent)**

- ▼ **SEL immune up to $121\text{MeV}\cdot\text{cm}^2/\text{mg}$ LET (Au ion)**
 - Tested **statically**, and in every dynamic operational mode

- ▼ **Fully functional after 2Mrad(Si) TID**
 - Bandgap shift increase with dynamic activity (from junction leakage)
 - No other ADC block shows any shift (proved by restoring VBGO)
 - No rebound – dynamic thermal anneal most efficient (back to <1%)
 - Performance vs. TID minimally affected: even with VBGO shift, observed up to **74.1dBFS SNR, 92dBc SFDR to 2Mrad(Si)**

- ▼ **Monitors 1 to 4 Power Supplies (or other System Signals)**
 - Timed output signals to sequence voltage regulators
 - Output signals can be programmed active-high or active-low
 - Timed RESET_B & RESET signals
 - Under-voltage thresholds: Pre-Set or User Defined
 - Over-voltage mode: 2-Channels monitored for BOTH under- and over-voltage conditions
 - MASTER_RESET_B pin allows for easy daisy-chaining to sequence more than 4 supplies

UT04VS33P Block Diagram



0.35 μm Triple-Well 4LM CMOS



| | |
|---------------------------------|--|
| Technology Type | 0.35 μm Mixed-Signal CMOS |
| Minimum Feature Size | 0.35 μm |
| Well Structure | Triple-Well (Substrate Isolated) |
| Transistors Used | 3.3V Enhancement Mode Isolated NMOS & PMOS (self-aligned) 5.0V Enhancement Mode Isolated NMOS & PMOS (self-aligned) Bipolar NPN (vertical) |
| Metallization and Interconnects | 4LM, Tungsten Plugs, CMP Planarization |
| Resistors | Diffusion Resistors, Poly Resistors (non-salicided), Hi-Poly Resistors |
| Capacitors | MiM, MOS-caps |
| Aeroflex Enhancements | RH OTEP Metal Fuse |

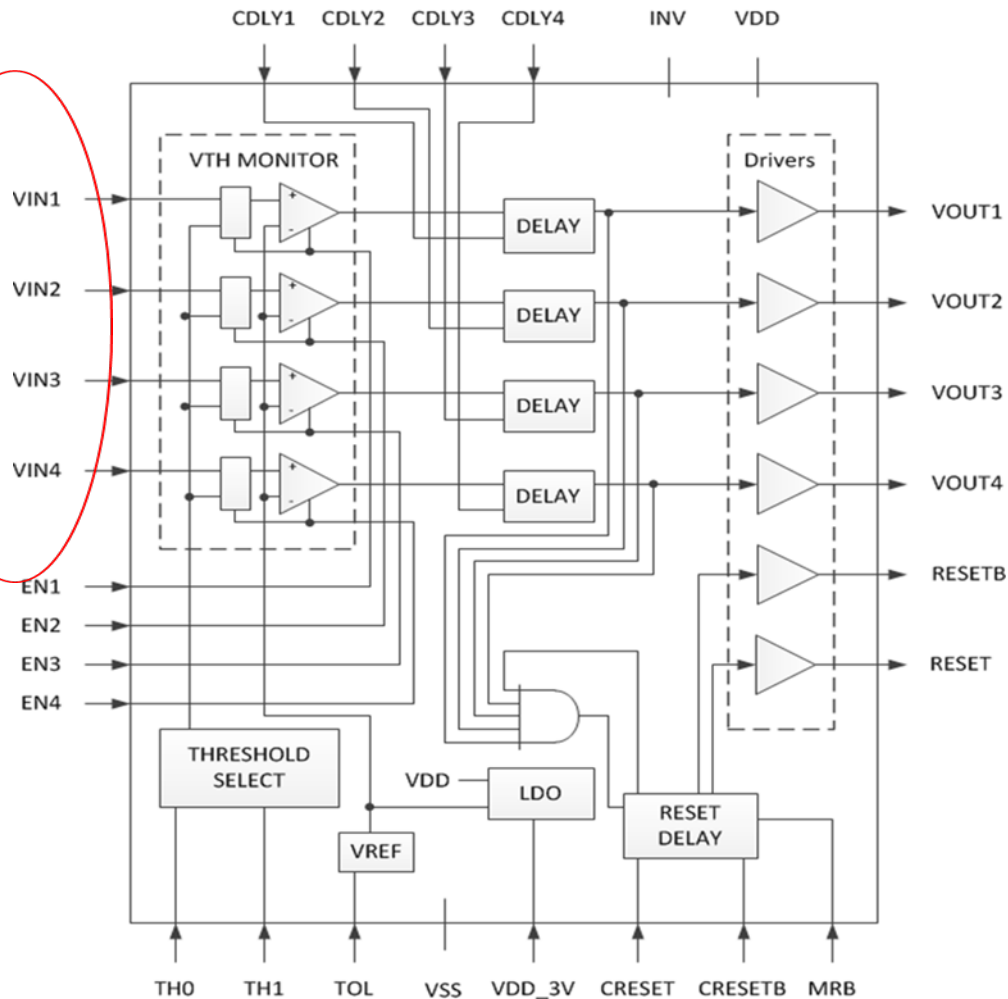
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Aeroflex RH Digital Library, I/O's, and Analog IP Blocks

QML-V New Technology Qualification: June 2012

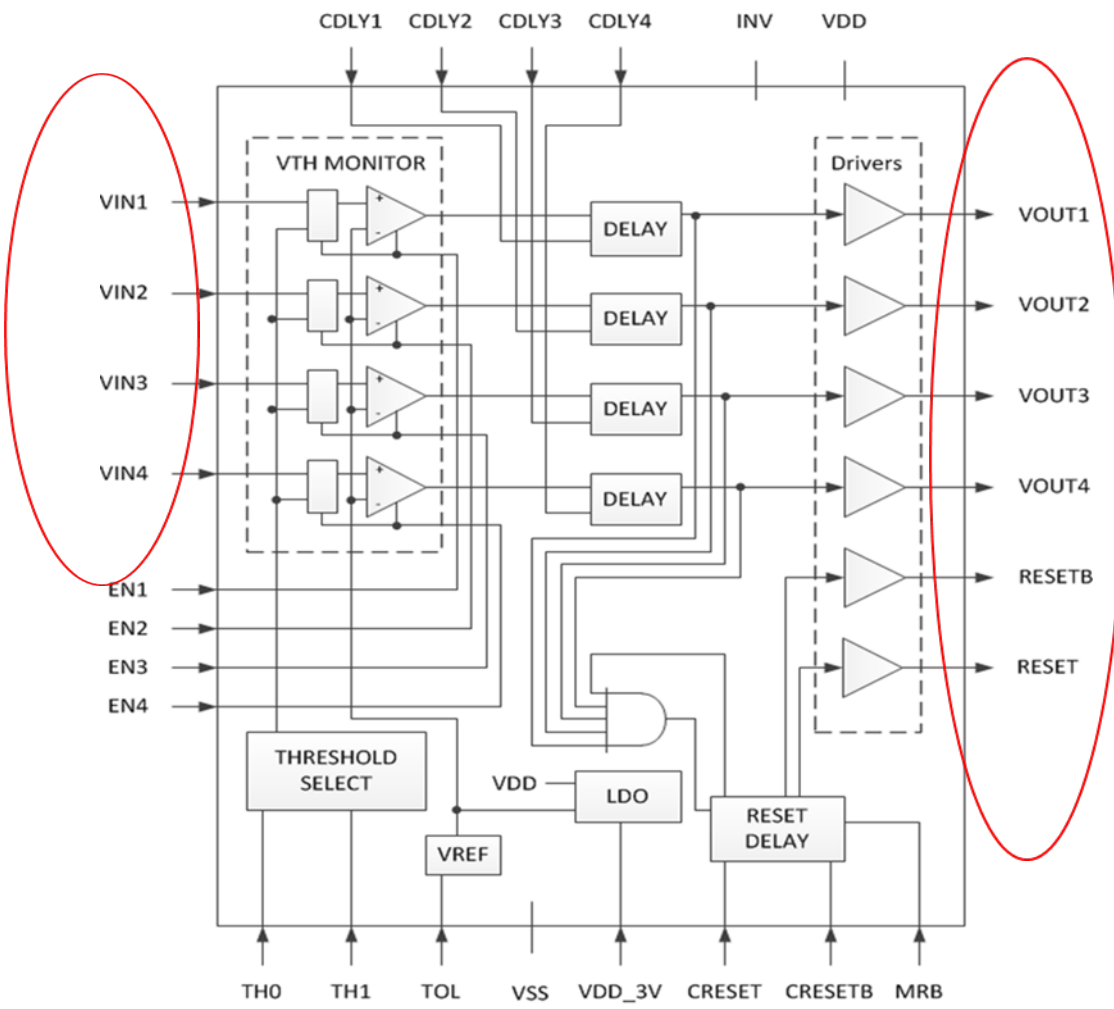
UT04VS33P Block Diagram

Inputs set to 50mV above comparator trip point



UT04VS33P Block Diagram

Inputs set to 50mV above comparator trip point



Outputs monitored for SET (either glitches or change in state)

▼ Asynchronous Part:

- 100% exposed to SET events: SET could cause inadvertent system RESET

▼ Tools Used:

- Qsim (Critical Charge) & SETsim (Rate vs Charge)

▼ Design Goal:

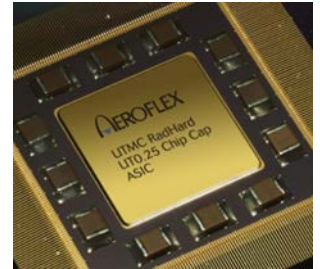
- No SETs below 80 MeV cm²/mg

▼ 1st Pass Silicon Success:

- 300krad(Si)
- No SETs with less than min. VDD (2.7V) at > 110 MeV cm²/mg for 4E7 ions/cm²

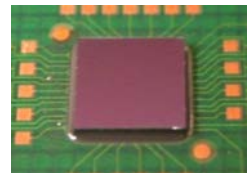
▼ Current Packaging Technology

- Hermetic ceramic packages from 12 to 377 user I/O, CQFP, CCGA
- PEM's: BGA (81 to 484 ball), QFN (12 to 28 pin), PQFP (40 to 208 pin), etc. in pitches ranging from 0.4 to 1.27 mm
- QML-V level external passive attach (resistor, capacitor)



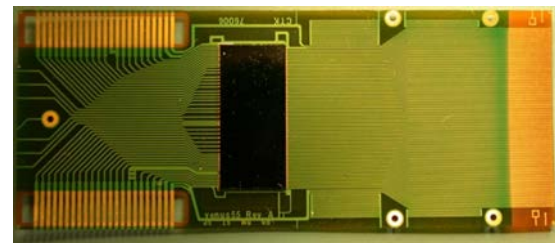
▼ Plug & SenseSM Packaging

- Flip Chip with Under Bump Metallurgy (UMB) and various underfills
- Flip-Chip on Flex, PCB, or Ceramic
- Hermetic photonic device packaging for space



▼ Advanced Packaging Technology

- Cantilever and Pyramid Stacked die
- CCGA Solder Column attachment
- Seam Sealing



Summary

▼ Aeroflex:

- Turn-Key Supplier for Radiation Hardened Mixed-Signal ASICs

▼ QML-V ASIC Technologies:

- 0.35 μm Triple-Well, 4LM BCD (3.3V up to 40V)
- 0.35 μm Triple-Well, 4LM CMOS (3.3V & 5V)
- 0.18 μm Triple-Well, 6-7LM CMOS (1.8V & 3.3V)

▼ Key Success Factors:

- 12 Years of Radiation Hardened Mixed-Signal ASIC Experience
- Extensive Analog IP Library: signal conditioning, data conversion, and actuation
- Modeling (Compact Transistor Models, SET Error Rates using Qsim/SETsim, Safe Operating Area using Hot Carrier Models TDDDB, and Electromigration Rules)
- In-House Radiation Test Facilities + Access to Heavy Ion, Proton, Nuclear Reactor Testing

Dank U!
Thank you!
Danke!
Merci!
Grazie!
Gracias!
Tack!
Ευχαριστούμε!
תודה!