

Author: Cesar Boatella Polo

Title: ASIC Radiation Testing Methodology and Techniques

Abstract:

ASIC devices are particularly interesting for space applications given their performance, size and power consumption. However, radiation qualification and testing is not straight forward due to their complexity, such devices may include a number of different functional blocks like memories (RAM and / or ROM), ADCs, DACs, signal amplifiers, signal processors etc. This complexity makes ASICs potentially sensitive to a wide range of radiation induced Single Events Effects (SEE, single events effects) and cumulative parametric degradation effects (TID and TNID, Total Ionising Dose and Total Non-Ionising Dose).

For instance, a mixed signal CMOS ASIC with digital and analog I/Os servicing a detector to read and amplify might be sensitive to TID, Single Event Effect Latch-up (SEL), Single Event Transient (SET) due to its analogue outputs and to Single Event Upsets (SEU) on its digital output registers. Such devices may also be sensitive to Single Event Functional Interrupt (SEFI) due to possible radiation sensitive state registers.

In this presentation the Radiation Hardness Assurance (RHA) processes related to irradiation characterisation will be covered. This will include radiation facility selection, relevant radiation effects, dose rate and bias. Additionally related standards and test guidelines will be referenced.