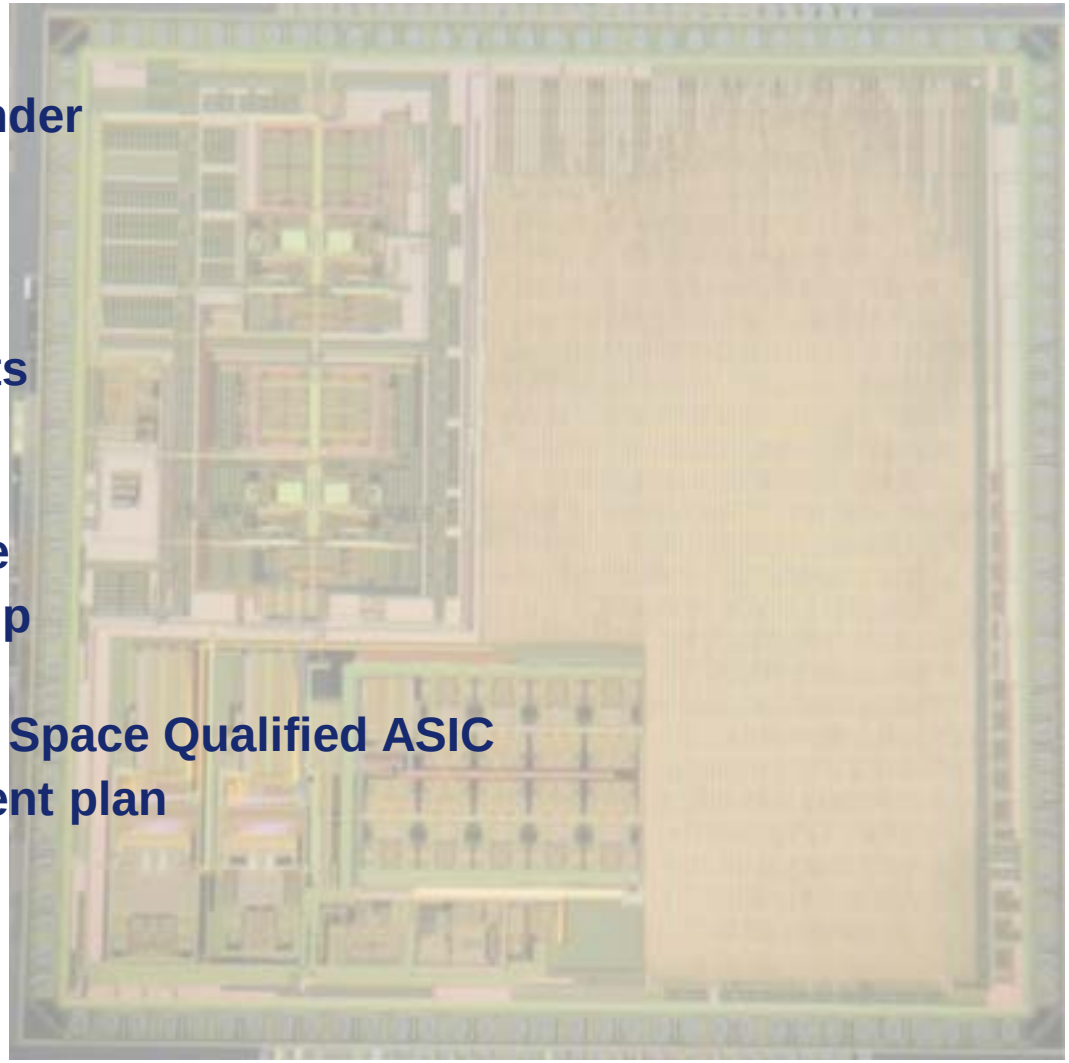
Electrical-Radiation test results of VASP and Flight Model Development Plan

Philippe AYZAC – THALES ALENIA SPACE

AGENDA



HIVAC / VASP project reminder

Electrical test results

- **Functional tests**
- **Characterization tests**

Radiation test results

- **Total Ionization Dose**
- **Single Event Latch-up**

From VASP prototypes to a Space Qualified ASIC

- **VASP FM Development plan**

Conclusion

HIVAC / VASP project reminder

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HIVAC / VASP project reminder

HIVAC project is an ESA co-funded project

- contract n°19872/06/NL/JA

Prime contractor : THALES ALENIA SPACE – France

- **Technical activity in HIVAC / VASP**
  - **Analog-Front-end and Top level design**
  - **Characterization tests**

Sub-contractors for :

- **ADC core design, Foundry, Prototype packaging**
- **EGSE design and functional tests, Radiation test**

Phase 1 : Specification - Architecture – Feasibility - Technology selection

- T0 : 07/2006 ADR VASP : 05/07/2007

Phase 2 : Detailed Design and Tests

- T0 : 11/2007 CDR VASP : 15/10/2009
- CDR EGSE VASP : 16/02/2010 TRR VASP : 07/07/2010
- Final presentation at ESTEC : 14/01/2011

HIVAC / VASP project reminder

VASP definition is focused on analog critical functions / specification :

Technology	Functional specification (2)	process)
Power Supply		
Power dissipation		
Analog functions	Technical specification (1)	
Pixel frequency	Radiometric specification (3)	
Input signal type		y
ADC resolution	16 bits	
Noise	< 2 Lsb	
ENOB	Radiation specification (4)	
DNL		
INL		
TID	Environmental specification (5)	
Latchup immunity		
Operational temperature range	-55°C to 125°C	
Full performance temperature range	0°C to 30°C	

HIVAC / VASP project reminder

Selected Technology :

XFAB XH035

CMOS 0.35µm

MLM foundry

Chip :

6.22mm X 6.21mm

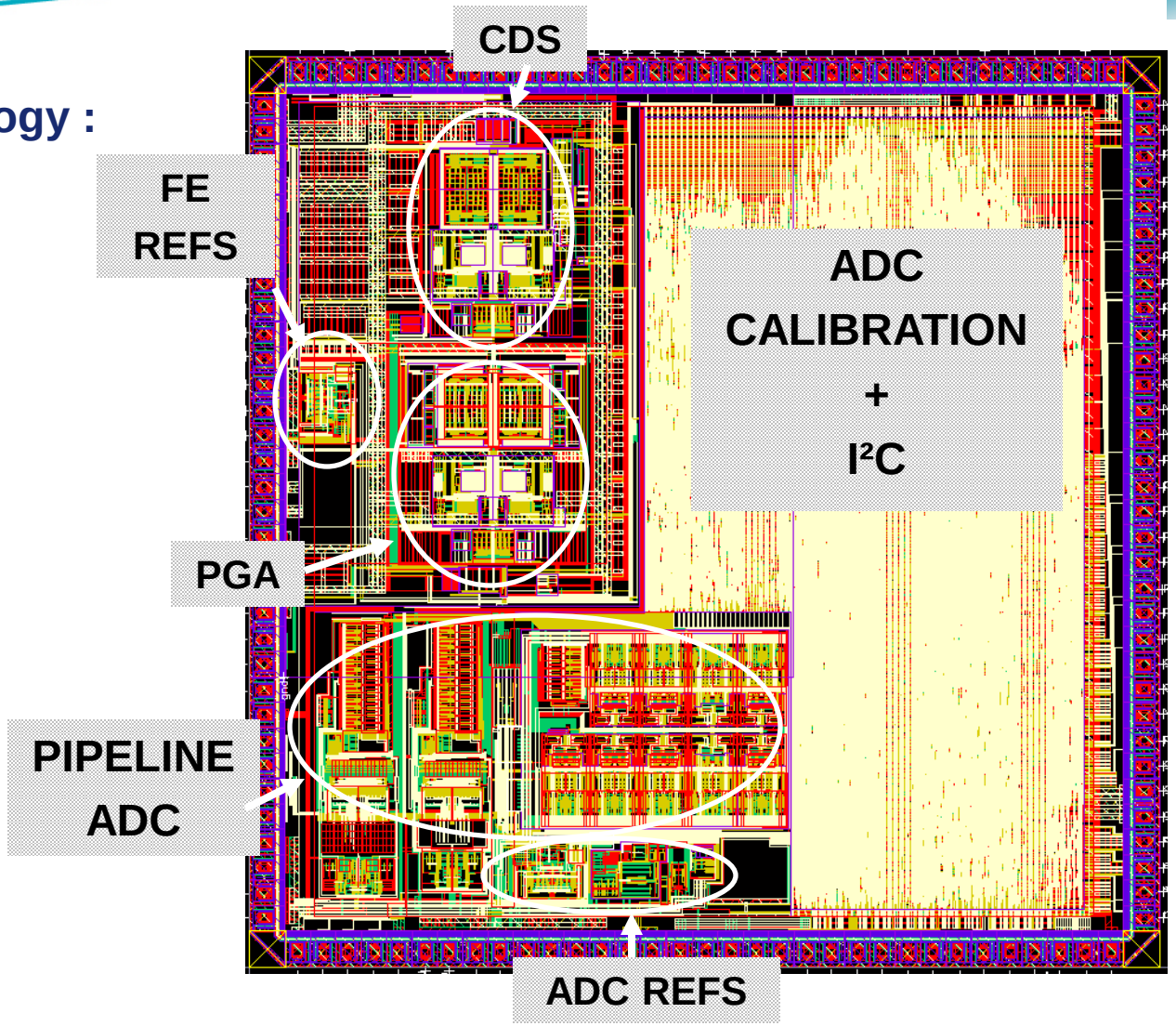
38.6mm²

132 IOs

Digital :

130k gates

9k gates/mm²



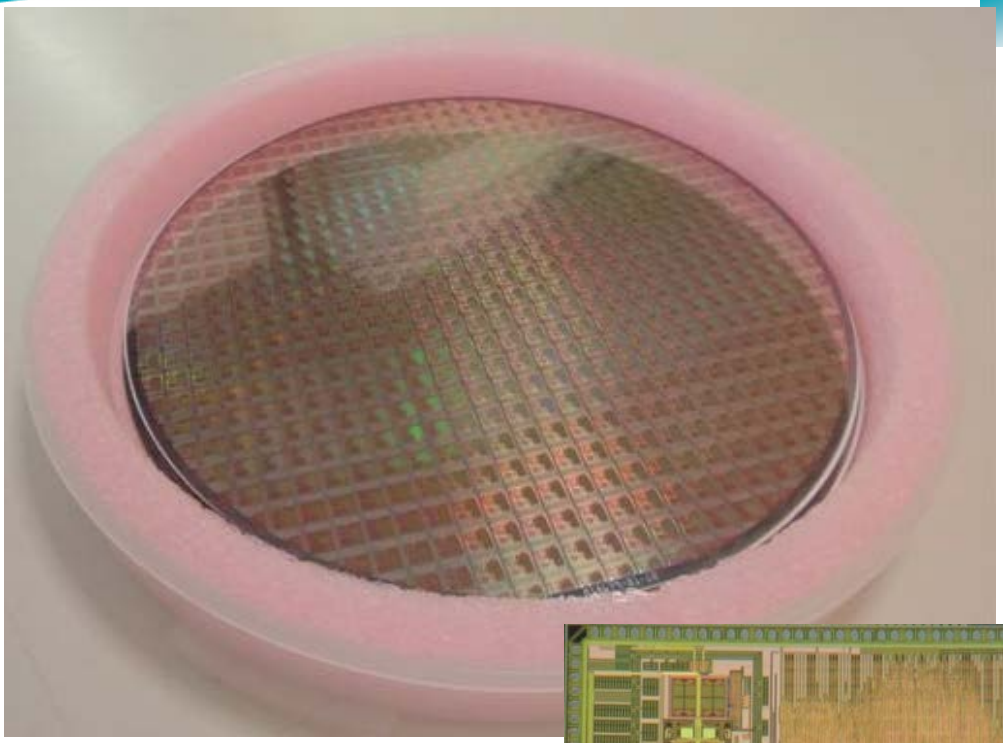
HIVAC / VASP project reminder

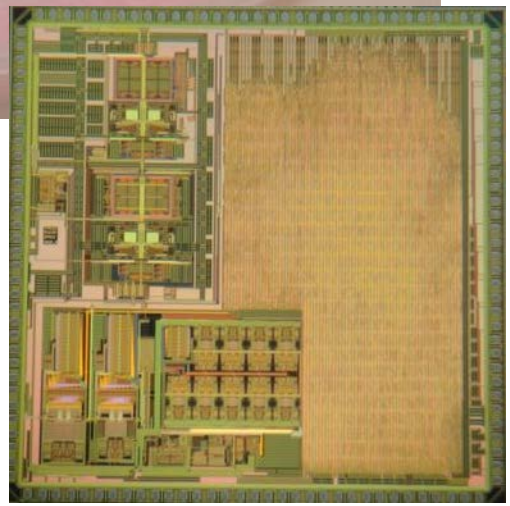
Analog-Front-End and ADC core are "Hardened by design"

Digital blocks are using not hardened XFAB standard cells

VASP prototype foundry (XFAB):

- **MLM 3 X 8" wafers**
- **450 VASP / wafer**
- **3 months manufacturing, delivery on time**
- **PCM available**





CQFP 132

Packaged by HCM in France

27 packaged prototypes

Electrical test results

HIVAC / VASP project reminder

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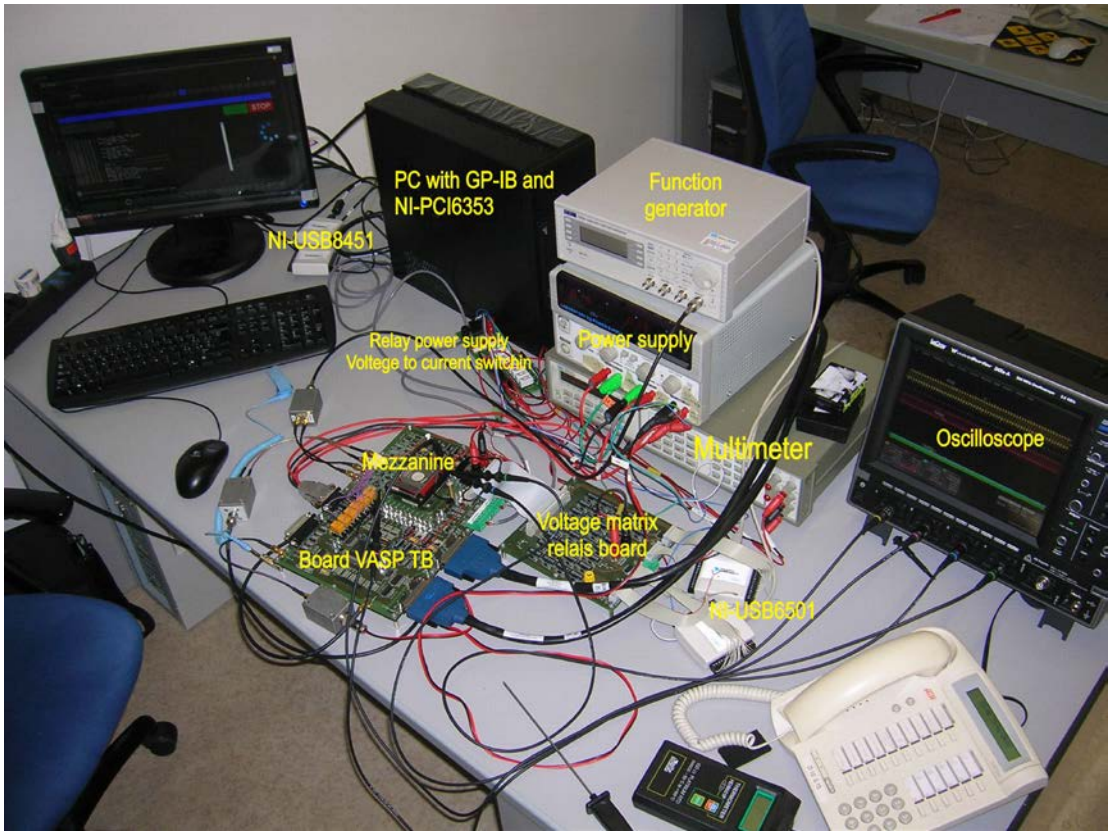
Functional tests

EGSE architecture for functional tests : -30°C to +80°C



Complete set-up

Detail:
VASP on mezzanine

Functional tests

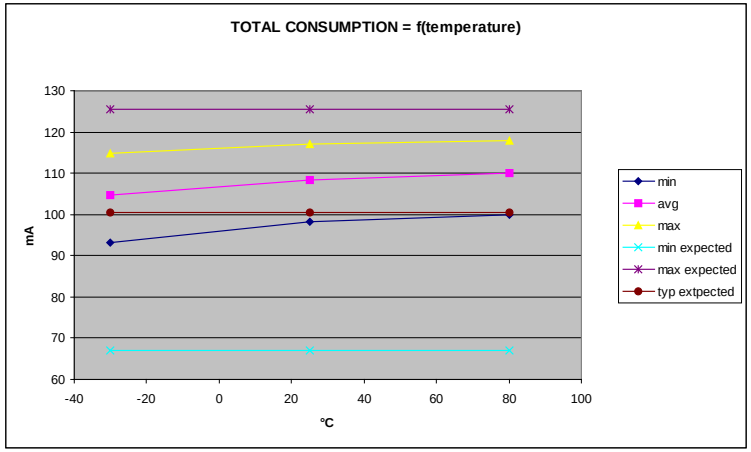
32 functional tests :

	20 Main Functional Tests
1	**Power supplies voltages**
2	**Static Current Consumption**
3	**DC voltages**
4	**References temperature slope trimming**
5	**References absolute value trimming**
6	**ADC calibration with nmean=0h**
7	**ADC calibration with nmean=3h**
8	**VASP in NORMAL mode with 0V differential CMOS signal**
9	**VASP in NORMAL mode with 1V differential CMOS signal**
10	**VASP in PGA BYPASSED mode with 0V differential CMOS signal**
11	**VASP in PGA BYPASSED mode with 1V differential CMOS signal**
12	**VASP in ADC ONLY mode with 0V differential CMOS signal**
13	**VASP in ADC ONLY mode with 1V differential CMOS signal**
14	**Fine offset injection**
15	**VASP in NORMAL mode with 0V pseudo-differential CMOS signal**
16	**PGA gain and coarse offset injection**
17	**CDS gain**
18	**VASP in NORMAL mode with 0V differential CCD signal**
19	**VASP in NORMAL mode with 1V pseudo-differential CCD signal**
20	**VASP multi sampling**
	5 Secondary Functional Tests
21	Default value of I²C registers
22	I2C address recognition
23	ADC calibration “expected value” tuning
24	ADC calibration coefficient via I²C
25	ADC request copy of ADC calibration coefficients to I²C calibration coefficients
	2 Manufacturing Tests
26	I2C link and I²C Registers glued bit
27	Scan chain
	5 Debug purpose Tests
28	Coarse Offset range and resolution
29	Fine Offset range and resolution
30	Access to VASP’s internal analog test points
31	ADC calibration in test mode
32	ADC in test mode

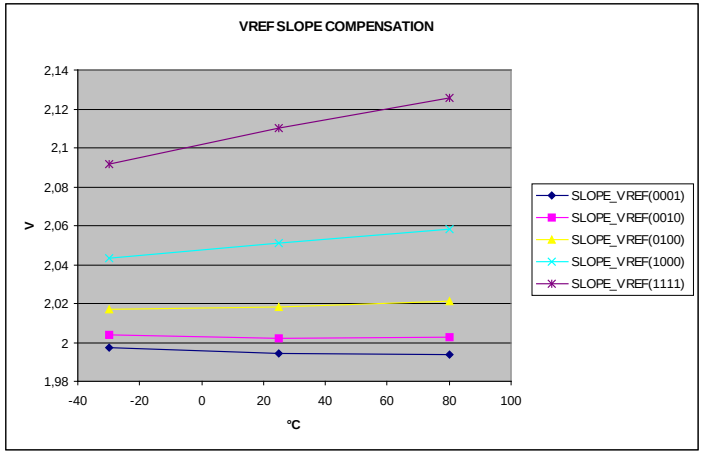
- **100% of VASP’s functionalities are validated : no functional bug in VASP design.**
- **100% of the functionalities are validated from –30°C to +80°C.**
- **Reference voltage buffer needs external stability compensation**
- **The packaging and electrical functional yield is 86.4% which is consistent with expectation for prototypes without Electrical Wafer Sort.**

Functional tests

VASP consumption :

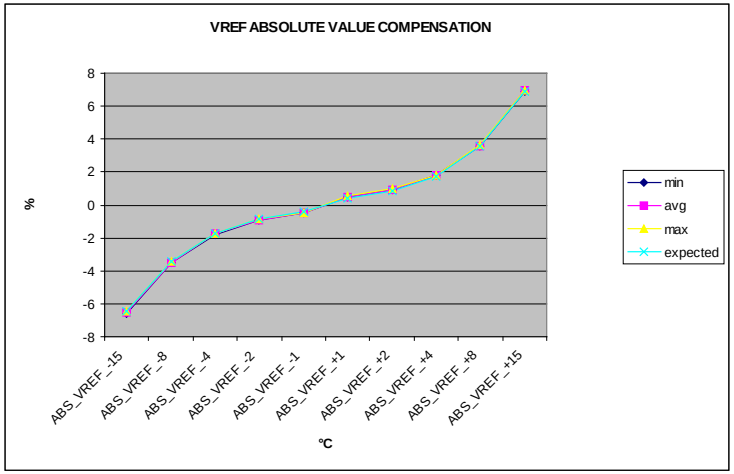


Reference voltage temperature slope tuning :



Access to internal analog nodes : ADC inputs

Reference voltage absolute value tuning :



Electrical test results

HIVAC / VASP project reminder

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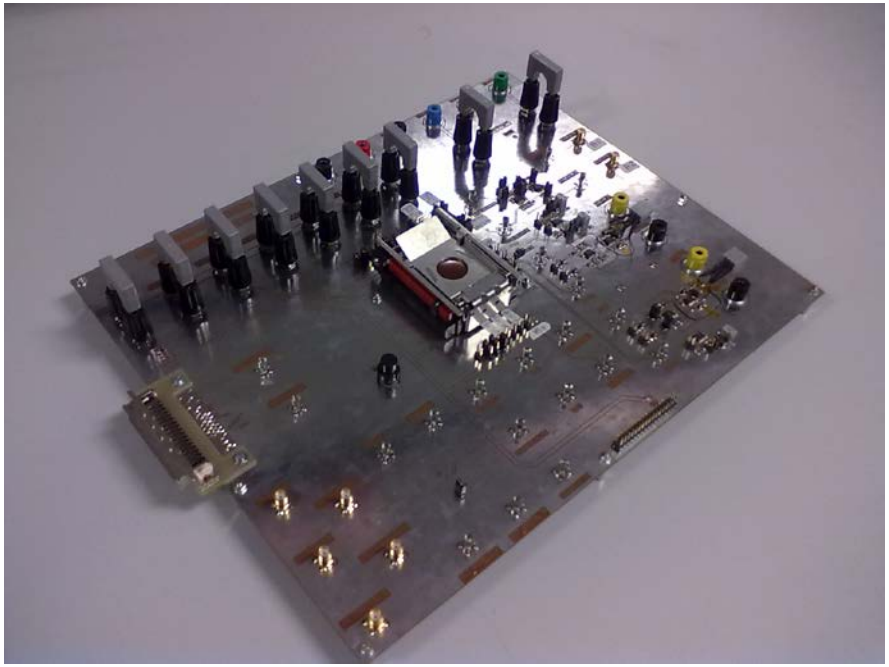
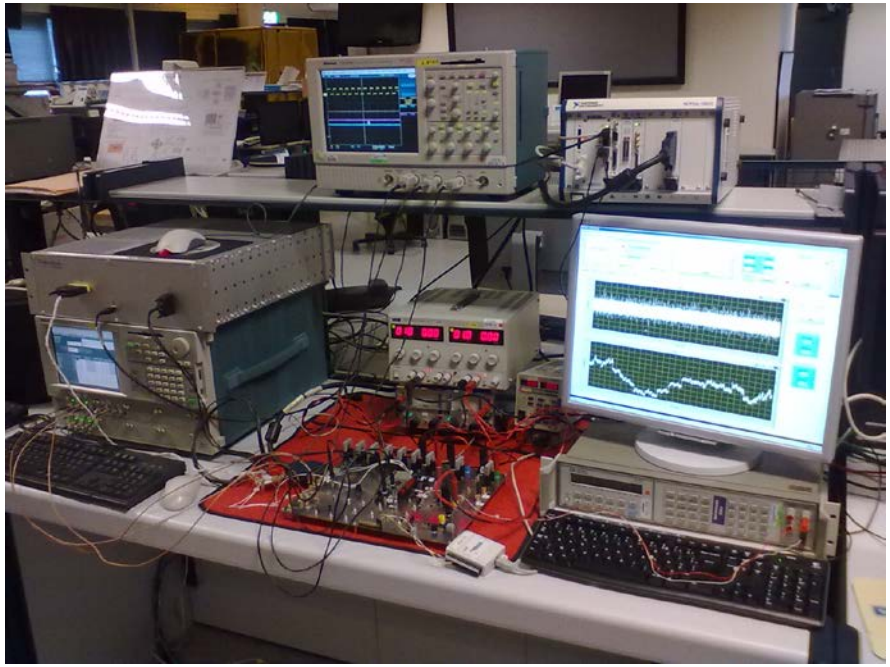
Characterization tests

Characterization board :



Characterization test-bench :



Focused on VASP's performances :

- Minimize parasitic
- Minimize coupling

Characterization tests

All Tests in TYPICAL conditions

CH

		Comment	Typ	WC Alim +/-5%	-30°C +25°C +80°C	Sensitivity +10°C +40°C	CCD / CMOS	VASP modes	X1 CDSX2 X8	X2,5, X3 X3,5, X4, X5, X6, X7	Freq 100k	Freq 1M	Freq 3M	Freq 6M	Calibration
1	Reference voltages		X	X	X	X									
2,1	noise nominal consumption	Channel 2 o													with
2,2	noise max consumption														with
															with
															with
															thout
															with
															with
															with
3,5	gain : with calibration. Max consumption														with
3,6	Differential : other gain (linearity): with calibration														with
4	input common mode rejection CMOS		X				X	NORMAL					X		with
5	Offsets														with
6	rejection of CCD sy														with
7	I²C coupling noise														with

CMOS and CCD

All MODES :

- NORMAL
- PGA BYPA
- ADC ONLY

Spec

Over

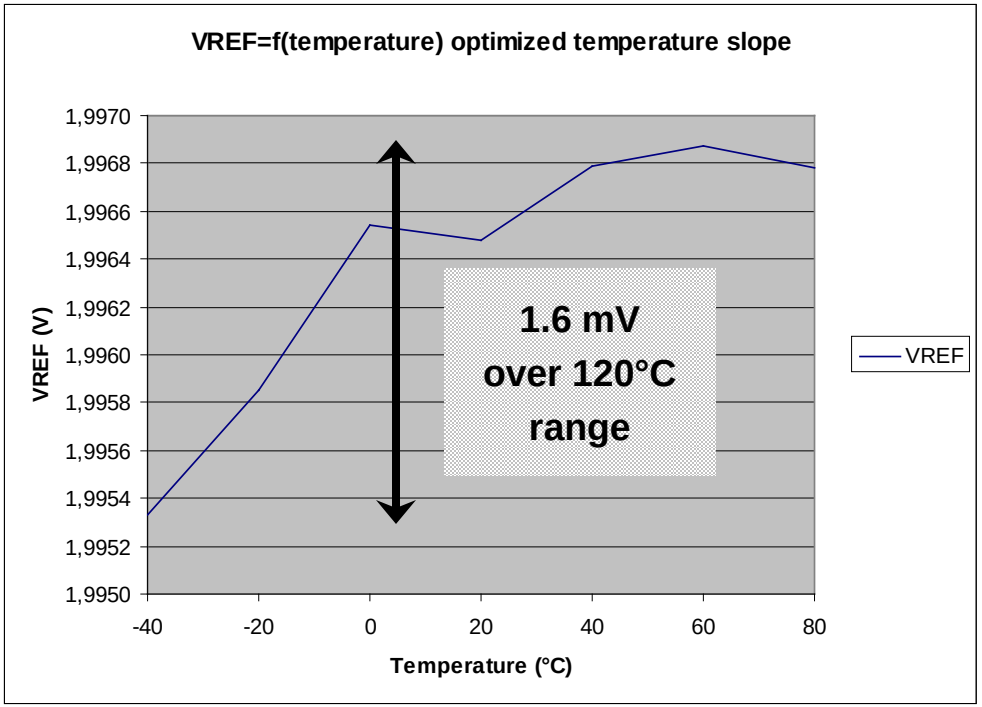
Characterization covers :

- Voltage references
- Noise
- Linearity
- Gain accuracy
- Static Input common mode rejection
- Offset
- Rejection of CCD synchronous noise
- I²C coupling noise

Main Tests from –30°C to +80°C

Characterization tests

REFERENCE THERMAL COEFICIENT :



THERMAL COEFICIENT :

Slope Register optimal value : 03dec

0 to +80°C : 120ppm (+1.5ppm/°C)

-40 to 0°C : 605ppm (+15ppm/°C)

Conclusion :

- **Temperature slope tuning operates as expected.**
- **Thermal drift can be tuned to accommodate the operational temperature range.**

Characterization tests

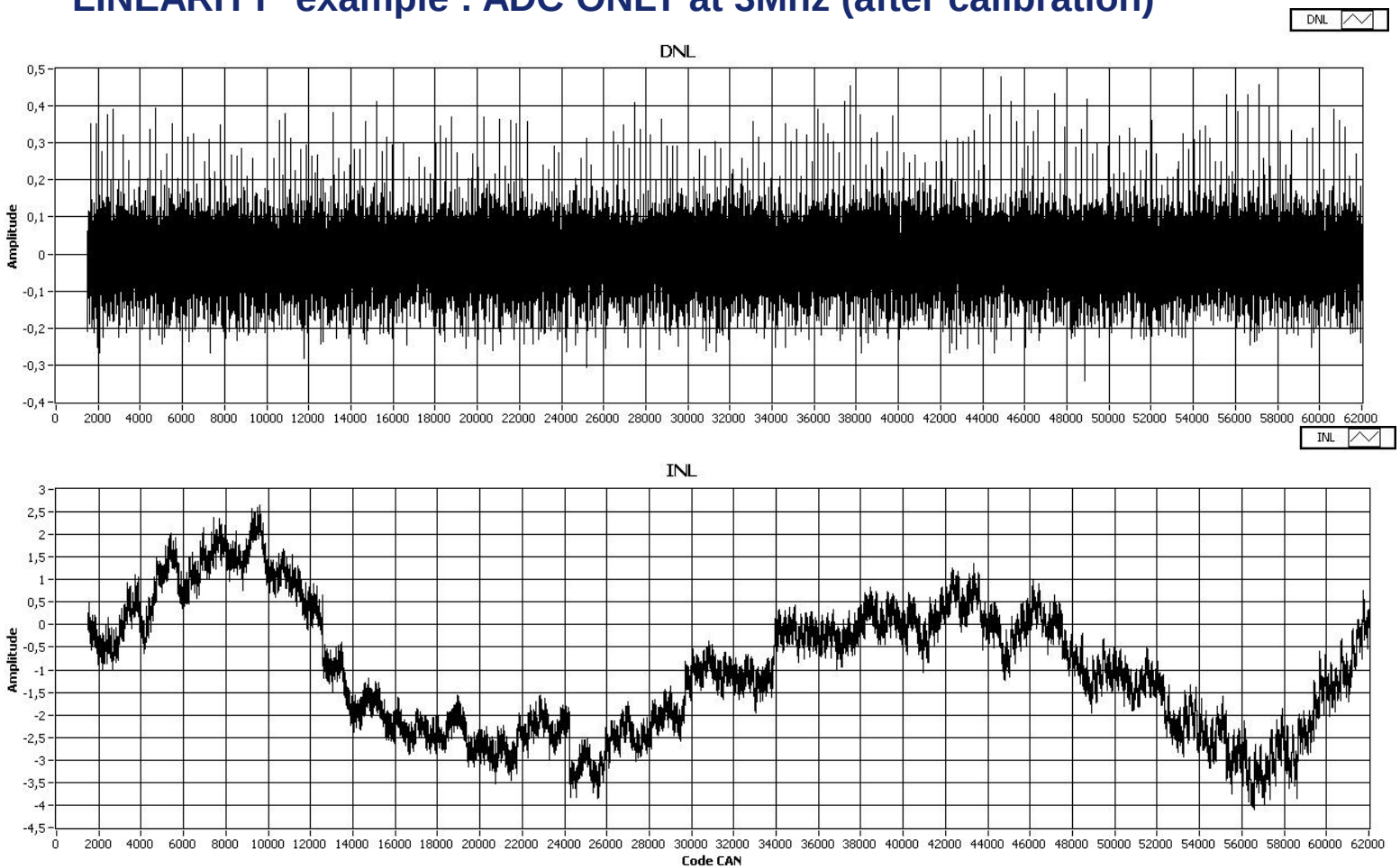
NOISE example : ADC ONLY at 3Mhz (after calibration)

NOISE NOMINAL CONSUMPTION			Input Referred Noise (lsb)			Max Expected Input Referred Noise @ 80°C
			25°C	80°C	-30°C	
CMOS	adc only	100kHz	0,8	0,8	0,7	1,1
		1MHz	0,8	0,8	0,7	
		3MHz	0,8	0,9	0,7	
		6MHz	1,1	1,6	1,1	

Noise conclusion :

- **Noise performance is as expected in ADC ONLY mode and PGA BYPASSED mode for CCD signal.**
- **In NORMAL mode (CDS + PGA + ADC), some noise degradation is induced by the front-end reference buffer stability.**
- **As ADC noise is particularly low, PGA does not provide Signal to Noise Ratio improvement.**

LINEARITY example : ADC ONLY at 3Mhz (after calibration)



Characterization tests

Despite :

- The Non Linearity of the Video Signal Generator does not allow to measure the ultimate linearity performances of VASP.
- Due to a foundry process problem in 2010 that is now fixed, the mismatch of the capacitors were increased by a factor of 8.7.

Linearity conclusion :

- **ADC has No missing codes**
- **DNL is as expected**
- **Calibration improves the ADC INL : DNL (-0.2 Lsb) and the INL (–6 Lsb)**
- **ADC INL and INL on CCD signal PGA BYPASSED mode are close to expectation.**

➢ Reference voltage generation stability has impact on linearity : it is particularly visible in CMOS mode, when PGA is used and on pseudo-differential signals.

Characterization tests

OTHER PERFORMANCES :

- ✓ **STATIC INPUT COMMON MODE REJECTION RATIO : not specified**
  - **CMOS MODE : 50dB**
  - **CCD MODE : 70dB**

- ✓ **GAIN ACCURACY : specification < 1%**
  - **CMOS & CCD : 0.6%**
  - **Reference voltage can be adjusted in a range of +/- 6.5%, step 0.4%.**

- ✓ **OFFSET : not specified**
  - **without calibration : < 6.2mV or < 100 Lsb**
  - **after calibration : < 62mV or < 1000 Lsb**

- ✓ **REJECTION OF CCD SYNCHRONOUS NOISE : not specified**
  - **> 80 dB**

- ✓ **I²C COUPLING NOISE :**
  - **Peak coupling of 25 Lsb during I²C communication**

Radiation test results

HIVAC / VASP project reminder

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- **Total Ionization Dose**
- ***Single Event Latch-up***

From VASP prototypes to a Space Qualified ASIC

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Conclusion

Total Ionization Dose

TID specific test bench.

2 dedicated boards :

- **For functional tests**
- **For radiometric characterization : noise and linearity**

Boards, test bench and TID campaign have been performed by TRAD.

Total Ionization Dose

Source :

- ^{60}Co at UCL, Louvain-La-Neuve (Belgium).

Dose rate :

- ESCC 22900 Low dose rate : 210 rad(Si)/hour .

Steps :

- 5krad, 10krad, 15krad, 19krad, 35krad.

Polarization types :

- ON sequenced, ON power shut down, fully OFF.

Stop at 35krad :

- Stopped due to a high drift on the consumption of the digital core designed with not hardened standard cells.
- Full recovery after annealing.

Total Ionization Dose

The TID campaign shows that :

- No miracle : the TID limit is resulting from the not hardened digital standard cells (digital consumption increase).
- All VASP samples are remaining fully functional at 35krad.
- The radiometric performances obtained at 35krad on hardened part of the design are showing no significant drift : no impact on noise, no impact on linearity, no impact on gain, very low drift of reference voltages.
- Polarization type (ON sequenced, ON power shut down, fully OFF) has no significant impact on drifts for the hardened parts of the design.

➢ **Thales Alenia Space "hardening by design" approach is validated**

➢ **Digital library needs hardening.**

Radiation test results

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Single Event Latch-up

SEL test has been performed on a representative test vehicle in the frame of an other activity :

- Cyclotron at UCL, Louvain-La-Neuve (Belgium).
- go-no-go test using Xenon ions (LET 67.7 MeV. cm²/mg).

All Hardened part of the design are SEL free :

- It validates the hardening by design approach used by TAS.

Not hardened parts (digital core cells and digital IO cells), are SEL sensitive :

- Digital library needs hardening.
- The VASP flight model shall use the hardened digital library (core and I/Os).

From VASP proto to a Space Qualified ASIC

HIVAC / VASP project reminder

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From VASP prototypes to a Space Qualified ASIC

- **VASP FM Development plan**

Conclusion

VASP FM Development plan

VASP FM (MTG mission)

- Validated VASP FM proto ADC core
- Hardening of Digital part

Tape-out : 12/2012

Wafer lot : 04/2013

Qualified parts : 08-09/2013

VASP FM prototype

- Spec changes : 4 MHz, PGA removal, clamp
- VASP FM proto ADC core digital hardening
- Improvement of references
- Digital part = not hardened VASP prototype digital part
- Goal : validation of new analog core performances

Tape-out : 07/2012

Prototypes : 10/2012

HIVAC / VASP prototype

- Good parametric results
- RADHARD to be completed for digital standard cells
- Improvement needed on voltage references

Digital library hardening

- Total ionizing dose
- SEL
- SEU

Available on 07/2012

2009 **2010** **2011** **2012** **2013**

VASP FM Development plan

Digital library hardening

- **The digital library cells are based on the VASP digital content and the content of a representative digital design (FIR ~100kgates) in test vehicle**

- **69 cells**
  - Combinational : 2 inputs, 3 inputs, inverted inputs, …
  - Buffer : size 2, 4, 6, 8
  - Flip-flop and latch: scan, complemented output, set, reset, …
  - Pads : supply, analog, digital

- **14 layout miscellaneous**
  - Filler cell
  - Filler cap
  - Antenna diode

➢ **Hardening principle**
- TID hardness is obtained by device design
- SEL hardness is obtained by layout
- SEU hardness is obtained by circuit design

VASP FM Development plan

- **Focus on DICE flip-flop : D**ual **I**nterlocked storage **CE**ll
  - Widely used SEU free technique for similar technologies
  - ESA Handbook : Techniques for Radiation Effects – Mitigation in ASICs and FPGAs (ESA-HB-XX-XX-rev.6)
  - Original white paper
    - Upset hardened memory design for submicron CMOS technology
    - Nicolaïdis, Calin, Velazco – IEEE 1996
  - Lot of publications on DICE. Specially usefull for this work :
    - Topology-related upset mechanisms in design hardened storage cells
      Nicolaïdis, Calin, Velazco – IEEE 1998
    - The 90 nm double-DICE storage element to reduce single-event upsets
      Haghi, Draper – IEEE 2009

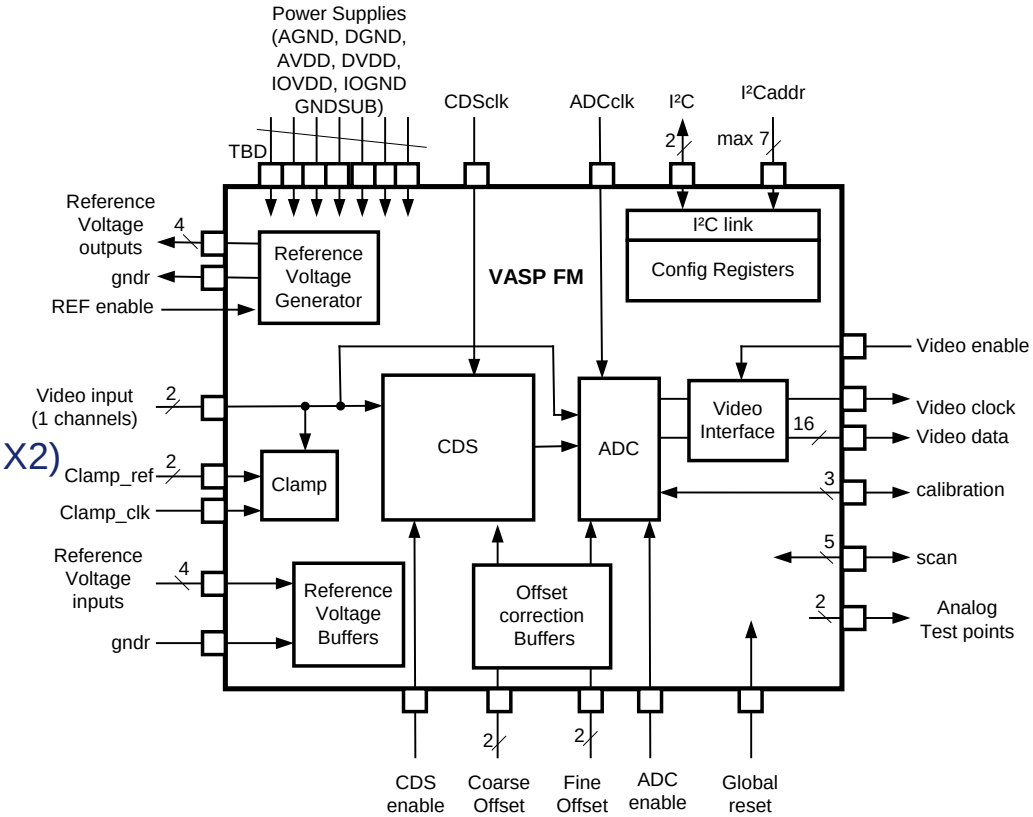
- **Support from CNRS/TIMA laboratory**
  - Peer review with DICE inventor and hardening experts
  - Schematic and layout review

VASP FM Development plan

VASP Improvements :

Analog blocks :

- Reference stability
- External reference capability
- Clamp
- Tri-state video data bus capability
- 4MHz pixel frequency
- Single input channel
- PGA suppressed (CDS gain X1 or X2)



Digital blocks :

- Use of Hardened Digital Cells

Radiation target :

- TID : 100 krad
- SEL : immune @ 70 MeV/mg/cm²
- SEU : 1.10^{-10} event per day per cell

VASP FM Development plan

Industrial organization for FM qualification and production :

- **Foundry : XFAB XH035**
  - ISO 9001:2000/2008
  - Automotive referential : ISO TS 16949:2002/2009
  - Customer alert via automated email
  - Wafer lot delivery with PCM

- **Back-end activities :**

✓ **ESCC Generic Specification No. 9000**
  - Partners are identified to cover all activities :
    - Packaging, Qualification, FM production
  - All of them have already experience in space integrated circuit manufacturing and qualification :
    - E2V, MICROSS, RF2M Microelectronics (ex C-MAC), SERMA, etc…

VASP FM Development plan

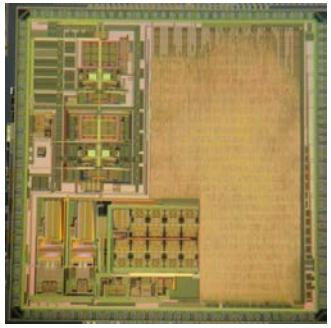
Qualification according to ESCC Generic Specification No. 9000

- Chart F 1 - General Flow chart for VASP ASIC procurement
- Chart F 2 - Production Control
- Chart F 3 - Screening Tests
- Chart F 4 - Qualification and Periodic Tests
- Chart 5 - Flow Chart for Radiation (TID) Qualification and Lot Acceptance Testing
- Chart 6 - Flow Chart for Radiation (SEE) Qualification and Lot Acceptance Testing

VASP could be delivered as qualified packaged component

Conclusion

- ✓ **High and ambitious level of electrical performances have been achieved**
- ✓ **Thales Alenia Space "hardening by design" approach is validated on the selected XFAB XH035 technology for TID and SEL**
  - ➢ **VASP FM will be fully hardened : TID, SEL and SEU**
- ✓ **VASP FM prototype foundry is on-going**
- ✓ **VASP FM digital part hardening is on-going**
- ✓ **VASP FM back-end organization is on-going**
  - ➢ **Qualified VASP FM expected by 08-09/2013**



Thank you for your attention

See you at AMICSA 2014
with MTG VASP FM tests and qualification results …

philippe.ayzac@thalesaleniaspace.com