AMICSA 2012
Mixed-Signal ASICs Development Methodology

28th August 2012

All the space you need

ASTRIUM
AN EADS COMPANY

Outline

INTRODUCTION

WHAT DO WE NEED ?

HERITAGE

PROCESS

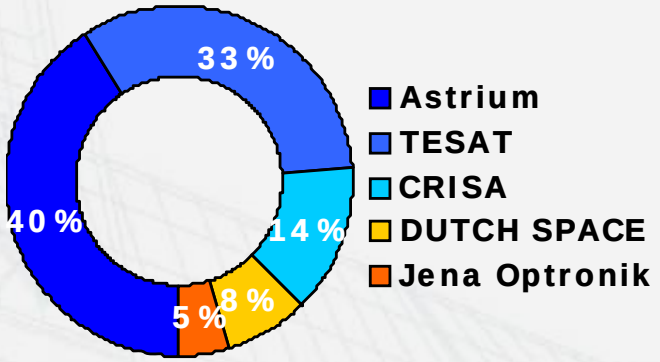
CONCLUSION

Astrium Product

2960 employees

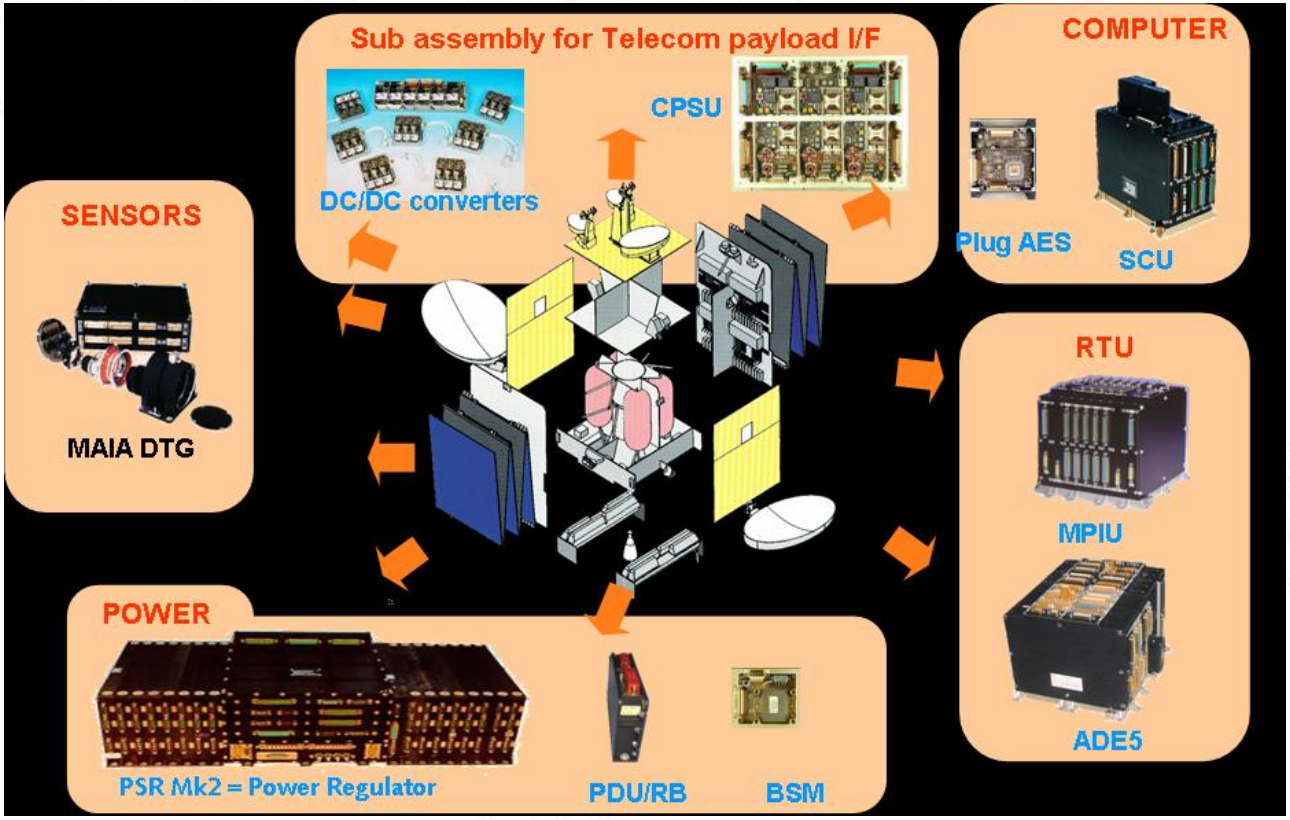
5 country, 10 sites

Business volume 600 M€



Astrium product in France: driven by Class 1 SatCom market

- Main activity for Eurostar 3000 and Alphabus platform
- 40 units and 350 modules to be delivered in 2012
- 1000 hybrids and MCM produced per year



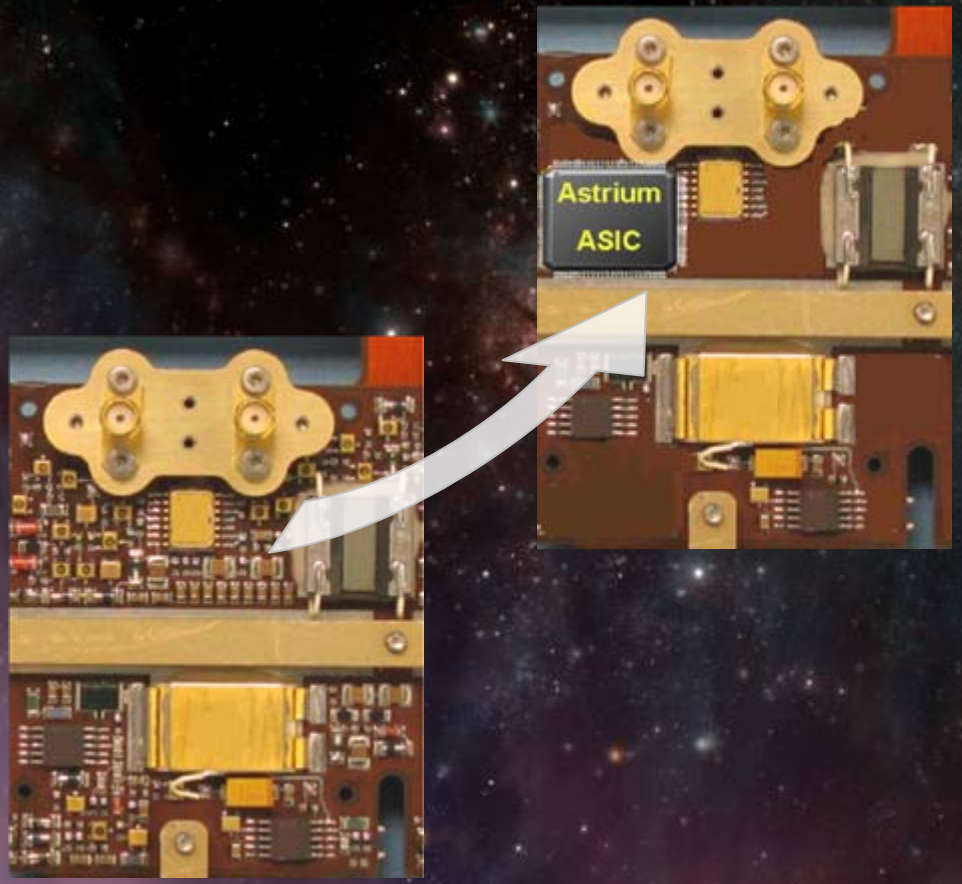
Introduction:
Benefits of analogue and mixed-signal ASICs

Mixed-Signal ASICs:

> Enable a high level of miniaturization

> Allow future satellites to offer more functionalities

> Are highly strategic to secure and improve Astrium's future business capability



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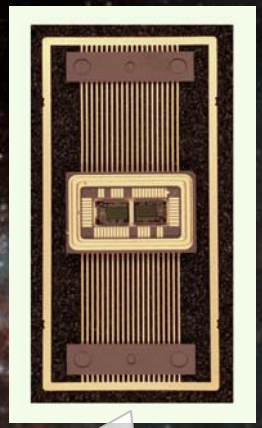
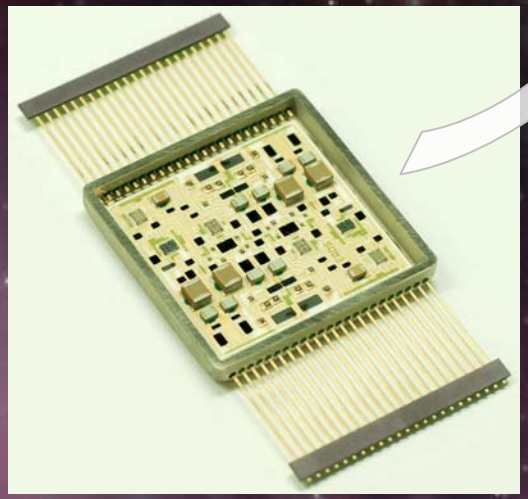
Introduction:
Benefits of analogue and mixed-signal ASICs

- Decreased Power Consumption
- Reduced Mass and Volume
- Fewer Components
- Better Performance
- Higher Reliability
- Improved Testability/Monitoring
- Enhanced Manufacturability
- More Functionalities
- Shorter Manufacturing Time
- Shorter Repair Time
- Higher Production Yield
- Lower Recurring Costs





Astrium's needs for mixed-signal ASICs

	Internal function	Max. Frequency	Logic Voltage	Analogue Voltage/Current/Power	Integration	Number/Year
1553 Transceiver 3V3/5V		1MHz max	3V3 / 5V	5V / 1A / 1W	Low	200
1553 Transceiver 3V3/15V		1MHz max	3V3 / 5V	15V / 0,3A / 1W	Low	1000
I/O handling in Data Management Systems	Digital bus, ADC Mux	Clock XMHz BW < 20kHz	3V3	5V or 3V / low consumption	Medium (>64 voltage channels; >64 temperature channels)	200 (5 platforms) + 50
DC/DC Converter and motor control	Digital loop, PWM Power MOS, Driver ADC/DAC NVM	Clock XMHz PWM < 1MHz BW < 50kHz	3V3	15V / 1A peak / 1W	High	200
TC matrix / high power command	Power MOS, Digital bus	Clock ? Static	3V3	40V / 1,5A / 2W	Low	350 (Mat 16X16 for 5 platforms)
Control loop for PCU	Digital and analogue loops Non Volatile Memory	Clock XMHz BW < 50kHz	3V3	5V (TBC) / 0,5W	High	20 (for 5 platforms)
Driving of power cells for PCU	PWM Digital bus Power MOS, Driver	Clock XMHz BW < 50kHz	3V3	15V / 1A peak / 1W	Medium	100 (for 5 platforms)
Power converter for RF emitter (EPC)	PWM Digital bus, Digital loop Power MOS, Driver, NVM	Clock XMHz BW < 50kHz	3V3	15V / 1A peak / 1W	High	200 / payload
Video Chain	CMOS/CCD sensors biasing, Amplification, ADC	Clock ~50MHz BWP < ~Few MHz		5V or 3V / low consumption	Medium	10

All units have a lifetime of 15 years and they must withstand 50 to 100 krad

Building-Block definition

- A Building-Block is an advanced and fully characterized analogue function.
- It is the equivalent of an IC in discrete electronics.
- It is composed of a schematic and a layout. The layout guarantees the behaviour.

	1553	Data mgt	DC/DC	TC mat	PCU
ASIC for LEO / GEO	GEO	GEO / LEO	GEO / LEO	GEO / LEO	GEO
Building-Blocks list					
SPI interface		✓	✓	✓	✓
ADC interface (no driver)		✓	✓	✓	
Voltage reference		✓	✓	✓	✓
Multiplexer		✓	✓	✓	✓
Opamp instrumentation		✓	✓		✓
12-bits DAC		✓	✓		✓
12-bits ADC		✓	✓		✓
Power MOS driver	✓		✓	✓	✓
Power MOS	✓		✓	✓	
Analogue PWM			✓		
Digital PWM			✓		
Internal oscillator		✓	✓		✓
Non Volatile Memory			✓		✓
Other digital BB					

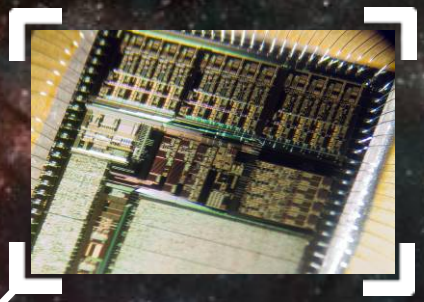
Future development

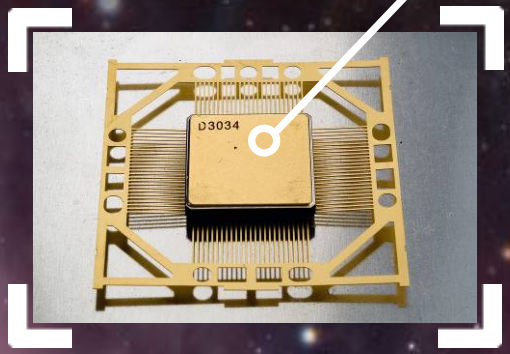
- To cover Astrium's needs over 10 years, the order of magnitude of 10 000 ASICs will be necessary.
- A industrial development methodology is needed to successfully develop these ASICs and to produce them properly.
- Astrium has the willingness to be involved in the harmonisation process

Astrium Heritage

Since 2000, Astrium has accumulated and implemented lessons learnt regarding mixed ASICs development

- Astrium used Atmel's technologies for digital ASIC since more than 20 years (0.5µm, 0.35µm, 0.18µm)
- Astrium has used XFab's 1µm SOI CMOS process with SITAEL since 2008 :
  - ESA contract of 1553 Europeanisation
  - Spanish 'Centro de Astrobiología' Contract in 2010 for NASA MSL mission (Mars)
- Astrium Tesat has used IMEC/UMC's 0.18µm CMOS (DARE) as well as LFoundry's 0.15µm CMOS processes
- Astrium used AMS's 1.2µm CMOS process





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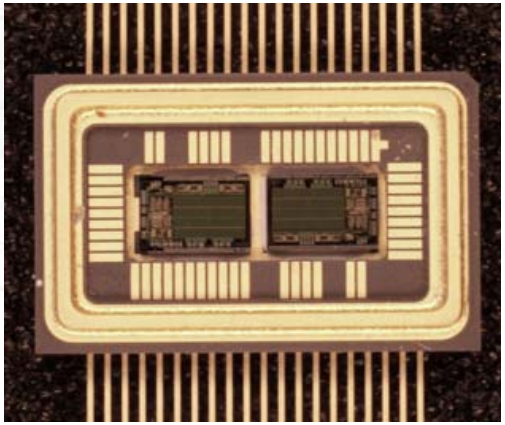
Heritage: the ADT822



- ADT822 is a 1553 tranceiver, to replace an hybrid
- It is developed to be a commercial component, like the SCOC3 for digital application
- Its development is ongoing
- Overall development process controled by Astrium Product, mastering space equipment from system design down to component manufacturing

Heritage:
Astrium's process for ADT822 development

- Development flow example:

The whole process is managed by Astrium

- Specification: Astrium
- Design & Layout: Design-House in charge of design, layout and foundry interface: Sitael
- Packaging design: Astrium
- Recurring test development: Astrium
- Wafer foundry: XFab
- Traceability and wafer sawing: HCM
- Wafer Test: None
- Packaging: Astrium
- Characterization: Astrium
- Recurring test: Astrium
- Qualification: Astrium

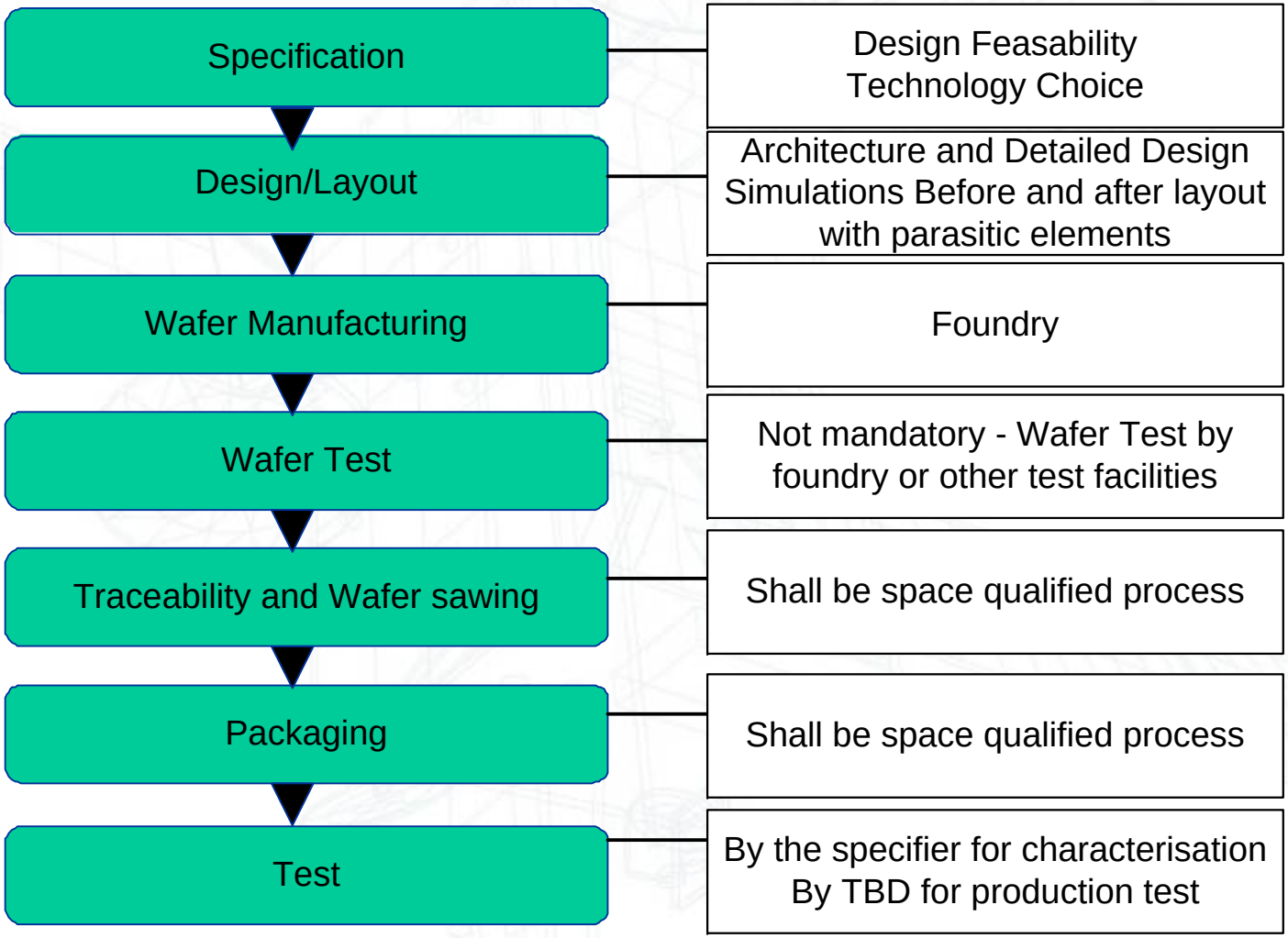
Development process

What we need now is:

- qualified complete industrial production flow;
- standardized development process/methodology;
- fully rad-hardened libraries (transistors, diodes, resistors, capacitors);
- simulation models (for transistors, diodes, resistors, capacitors) taking into account TID and ageing;
- fully characterized Building-Blocks with TID and ageing behaviour.

➔ Need for a few technologies and libraries to develop more complex ASICs.

Process:
Development and production flow



Process:
The actors

- The Final User/specifier, equipment designer
- The Design House
- The Foundery
- The Assembly and Test House

- The agencies for harmonisation and industry support

Process: Specification

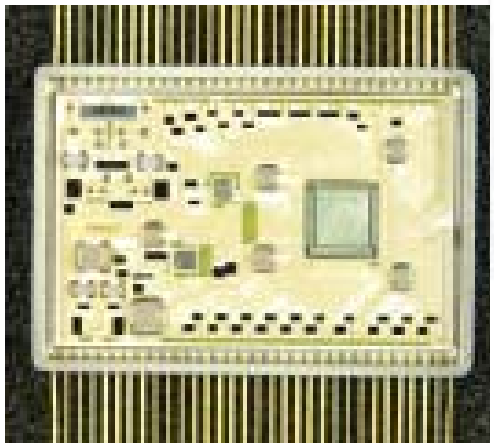
- Written by user
- The proximity of the user with the satellite system designers is key to optimize the system cost optimization
- Concurrent engineering with design-house to reach a compromise between ASIC contents and performance, risks mitigation and technology capability.

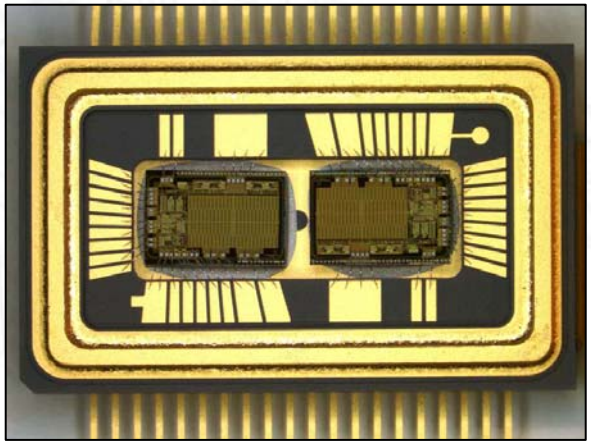
Process:
Design - Layout

- The design-house is responsible for the design, although a co-design between the User/Specifier and the design-house is needed
- Why a co-design:
  - Different approaches, points of view, concerns are beneficial for design quality. The user is rather concerned by system aspects, interactions with the outside, failure cases, ASIC architecture, *etc.* whereas the design-house is rather concerned by micro-electronic aspects and layout, building-blocks development, *etc.*
  - For schematics or schematics+layout, dual verifications lead to an improved design filter.

Process:
Assembly and Test House

- The choice of a space qualified Assembly and Test House compliant with the most demanding market is mandatory to simplify the development troubleshooting and to guarantee the perenity
- The packaging is part of the performances
- To select an already ECSS qualified production line is a security (Astrium Elancourt production line is used for ADT822)

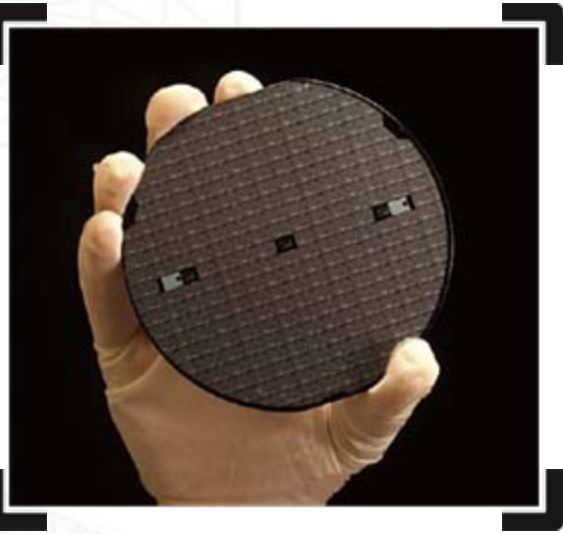




Conclusion

Agency support for:

- Selection of design house/founder compliant with european space needs
- Development and improvement of rad-hardened library;
- Development of simulations models taking into account TID and ageing;
- Development of fully characterized Building-Blocks;
- Standardization of development flow



➔ to make it work

➔ to give confidence to our customer

Thank you for your attention

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