AMICSA 2012
Mixed-Signal ASICs
Development Methodology

28th August 2012

All the space you need
2960 employees
5 country, 10 sites

Business volume 600 M€
Astrium product in France: driven by Class 1 SatCom market

- Main activity for Eurostar 3000 and Alphabus platform
- 40 units and 350 modules to be delivered in 2012
- 1000 hybrids and MCM produced per year
Introduction:
Benefits of analogue and mixed-signal ASICs

Mixed-Signal ASICs:
> Enable a high level of miniaturization
> Allow future satellites to offer more functionalities
> Are highly strategic to secure and improve Astrium’s future business capability
Introduction:
Benefits of analogue and mixed-signal ASICs

- Decreased Power Consumption
- Reduced Mass and Volume
- Fewer Components
- Better Performance
- Higher Reliability
- Improved Testability/Monitoring
- Enhanced Manufacturability
- More Functionalities
- Shorter Manufacturing Time
- Shorter Repair Time
- Higher Production Yield
- Lower Recurring Costs
# Astrium’s needs for mixed-signal ASICs

<table>
<thead>
<tr>
<th>Internal function</th>
<th>Max. Frequency</th>
<th>Logic Voltage</th>
<th>Analogue Voltage/Current/Power</th>
<th>Integration</th>
<th>Number/Year</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1553 Transceiver 3V3/5V</strong></td>
<td>1MHz max</td>
<td>3V3 / 5V</td>
<td>5V / 1A / 1W</td>
<td>Low</td>
<td>200</td>
</tr>
<tr>
<td><strong>1553 Transceiver 3V3/15V</strong></td>
<td>1MHz max</td>
<td>3V3 / 5V</td>
<td>15V / 0.3A / 1W</td>
<td>Low</td>
<td>1000</td>
</tr>
<tr>
<td><strong>I/O handling in Data Management Systems</strong></td>
<td>Digital bus, ADC, Mux</td>
<td>Clock XMHz BW &lt; 20kHz</td>
<td>3V3</td>
<td>Medium (&gt;64 voltage channels; &gt;64 temperature channels)</td>
<td>200 (5 platforms) + 50</td>
</tr>
<tr>
<td><strong>DC/DC Converter and motor control</strong></td>
<td>Digital loop, PWM Power MOS, Driver ADC/DAC NVM</td>
<td>Clock XMHz PWM &lt; 1MHz BW &lt; 50kHz</td>
<td>3V3</td>
<td>15V / 1A peak / 1W</td>
<td>High</td>
</tr>
<tr>
<td><strong>TC matrix / high power command</strong></td>
<td>Power MOS, Digital bus, Clock ? Static</td>
<td>3V3</td>
<td>40V / 1.5A / 2W</td>
<td>Low</td>
<td>350 (Mat 16X16 for 5 platforms)</td>
</tr>
<tr>
<td><strong>Control loop for PCU</strong></td>
<td>Digital and analogue loops Non Volatile Memory</td>
<td>Clock XMHz BW &lt; 50kHz</td>
<td>3V3</td>
<td>5V (TBC) / 0.5W</td>
<td>High</td>
</tr>
<tr>
<td><strong>Driving of power cells for PCU</strong></td>
<td>PWM Digital bus Power MOS, Driver</td>
<td>Clock XMHz BW &lt; 50kHz</td>
<td>3V3</td>
<td>15V / 1A peak / 1W</td>
<td>Medium</td>
</tr>
<tr>
<td><strong>Power converter for RF emitter (EPC)</strong></td>
<td>PWM Digital bus, Digital loop Power MOS, Driver, NVM</td>
<td>Clock XMHz BW &lt; 50kHz</td>
<td>3V3</td>
<td>15V / 1A peak / 1W</td>
<td>High</td>
</tr>
<tr>
<td><strong>Video Chain</strong></td>
<td>CMOS/CCD sensors biasing Amplification, ADC</td>
<td>Clock ~50MHz BW &lt; ~Few MHz</td>
<td>5V or 3V / low consumption</td>
<td>Medium</td>
<td>10</td>
</tr>
</tbody>
</table>

All units have a lifetime of 15 years and they must withstand 50 to 100 krad
A Building-Block is an advanced and fully characterized analogue function.

It is the equivalent of an IC in discrete electronics.

It is composed of a schematic and a layout. The layout guarantees the behaviour.

<table>
<thead>
<tr>
<th>Building-Blocks list</th>
<th>1553</th>
<th>Data mgt</th>
<th>DC/DC</th>
<th>TC mat</th>
<th>PCU</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIC for LEO / GEO</td>
<td>GEO</td>
<td>GEO / LEO</td>
<td>GEO / LEO</td>
<td>GEO / LEO</td>
<td>GEO</td>
</tr>
<tr>
<td>SPI interface</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>ADC interface (no driver)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Voltage reference</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Multiplexer</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Opamp instrumentation</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>12-bits DAC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>12-bits ADC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Power MOS driver</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Power MOS</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Analogue PWM</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Digital PWM</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Internal oscillator</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Non Volatile Memory</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Other digital BB</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
Future development

- To cover Astrium’s needs over 10 years, the order of magnitude of 10,000 ASICs will be necessary.
- A industrial development methodology is needed to successfully develop these ASICs and to produce them properly.
- Astrium has the willingness to be involved in the harmonisation process.
Astrium Heritage

Since 2000, Astrium has accumulated and implemented lessons learnt regarding mixed ASICs development

- Astrium used Atmel’s technologies for digital ASIC since more than 20 years (0.5µm, 0.35µm, 0.18µm)
- Astrium has used XFab’s 1µm SOI CMOS process with SITAEL since 2008:
  - ESA contract of 1553 Europeanisation
  - Spanish ‘Centro de Astrobiología’ Contract in 2010 for NASA MSL mission (Mars)
- Astrium Tesat has used IMEC/UMC’s 0.18µm CMOS (DARE) as well as LFoundry’s 0.15µm CMOS processes
- Astrium used AMS’s 1.2µm CMOS process
Heritage: the ADT822

> ADT822 is a 1553 tranceiver, to replace an hybrid

> It is developed to be a commercial component, like the SCOC3 for digital application

> Its development is ongoing

> Overall development process controled by Astrium Product, mastering space equipment from system design down to component manufacturing
Heritage: Astrium’s process for ADT822 development

Development flow example:
The whole process is managed by Astrium

- Specification: Astrium
- Design & Layout: Design-House in charge of design, layout and foundry interface: Sitael
- Packaging design: Astrium
- Recurring test development: Astrium
- Wafer foundry: XFab
- Traceability and wafer sawing: HCM
- Wafer Test: None
- Packaging: Astrium
- Characterization: Astrium
- Recurring test: Astrium
- Qualification: Astrium
Development process

What we need now is:

> qualified complete industrial production flow;
> standardized development process/methodology;
> fully rad-hardened libraries (transistors, diodes, resistors, capacitors);
> simulation models (for transistors, diodes, resistors, capacitors) taking into account TID and ageing;
> fully characterized Building-Blocks with TID and ageing behaviour.

Need for a few technologies and libraries to develop more complex ASICs.
Traceability and Wafer sawing

Design/Layout

Wafer Manufacturing

Wafer Test

Specification

Design Feasability
Technology Choice

Architecture and Detailed Design
Simulations Before and after layout
with parasitic elements

Foundry

Not mandatory - Wafer Test by
foundry or other test facilities

Shall be space qualified process

Shall be space qualified process

By the specifier for characterisation
By TBD for production test

Process:
Development and production flow

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Process: The actors

> The Final User/specifier, equipment designer
> The Design House
> The Foundery
> The Assembly and Test House

> The agencies for harmonisation and industry support
Process: Specification

- Written by user
- The proximity of the user with the satellite system designers is key to optimize the system cost optimization
- Concurrent engineering with design-house to reach a compromise between ASIC contents and performance, risks mitigation and technology capability.
The design-house is responsible for the design, although a co-design between the User/Specifier and the design-house is needed.

Why a co-design:

- Different approaches, points of view, concerns are beneficial for design quality. The user is rather concerned by system aspects, interactions with the outside, failure cases, ASIC architecture, etc. whereas the design-house is rather concerned by micro-electronic aspects and layout, building-blocks development, etc.

- For schematics or schematics+layout, dual verifications lead to an improved design filter.
The choice of a space qualified Assembly and Test House compliant with the most demanding market is mandatory to simplify the development troubleshooting and to guarantee the perenity.

The packaging is part of the performances.

To select an already ECSS qualified production line is a security (Astrium Elancourt production line is used for ADT822).
Conclusion

Agency support for:

> Selection of design house/founder compliant with european space needs
> Development and improvement of rad-hardened library;
> Development of simulations models taking into account TID and ageing;
> Development of fully characterized Building-Blocks;
> Standardization of development flow

⇒ to make it work
⇒ to give confidence to our customer
Thank you for your attention