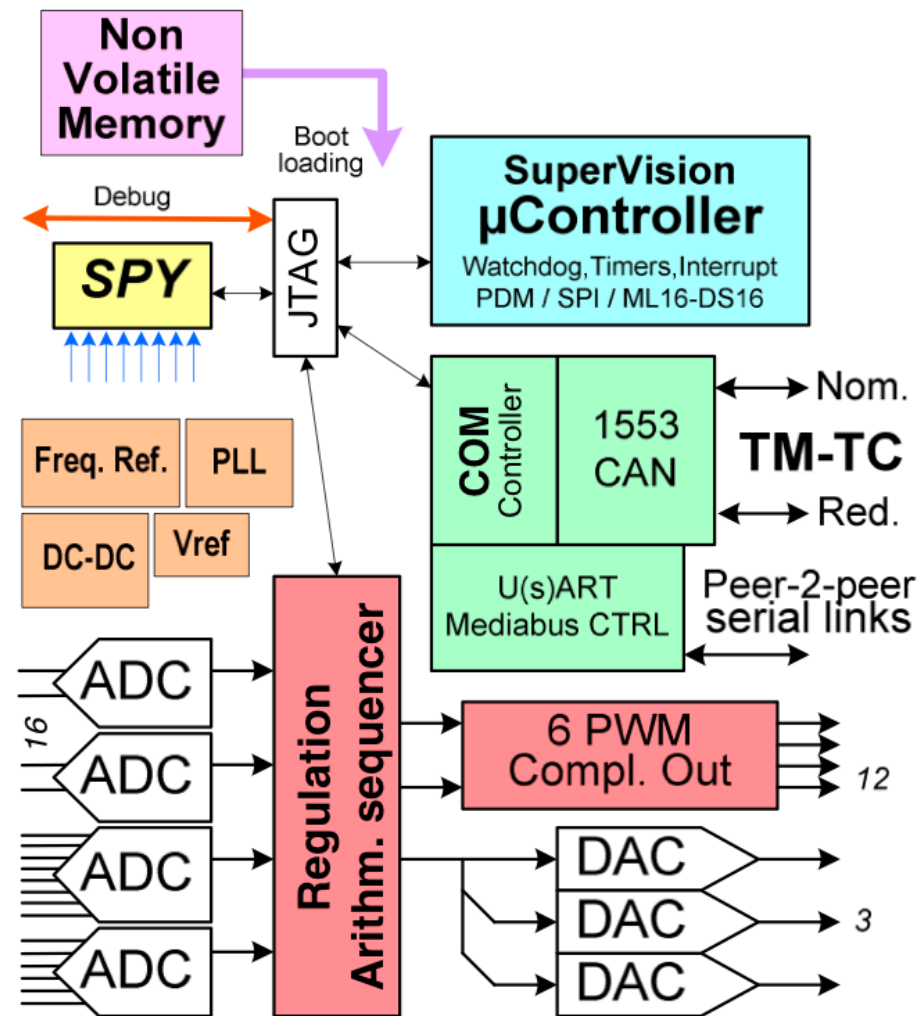


SOC: Digital programmable controller

- SOC currently in design phase
- Digital: 4 MCU cores
 - Supervision and management
 - Regulation arithmetic sequencer
 - Communication protocols
 - Debugging interface
- Analog
 - Reference voltage
 - Power management LDOs
 - Frequency reference
 - 4 flexible ADC
 - 3 DACs
 - PWM
 - POR circuitry
 - Under voltage detector



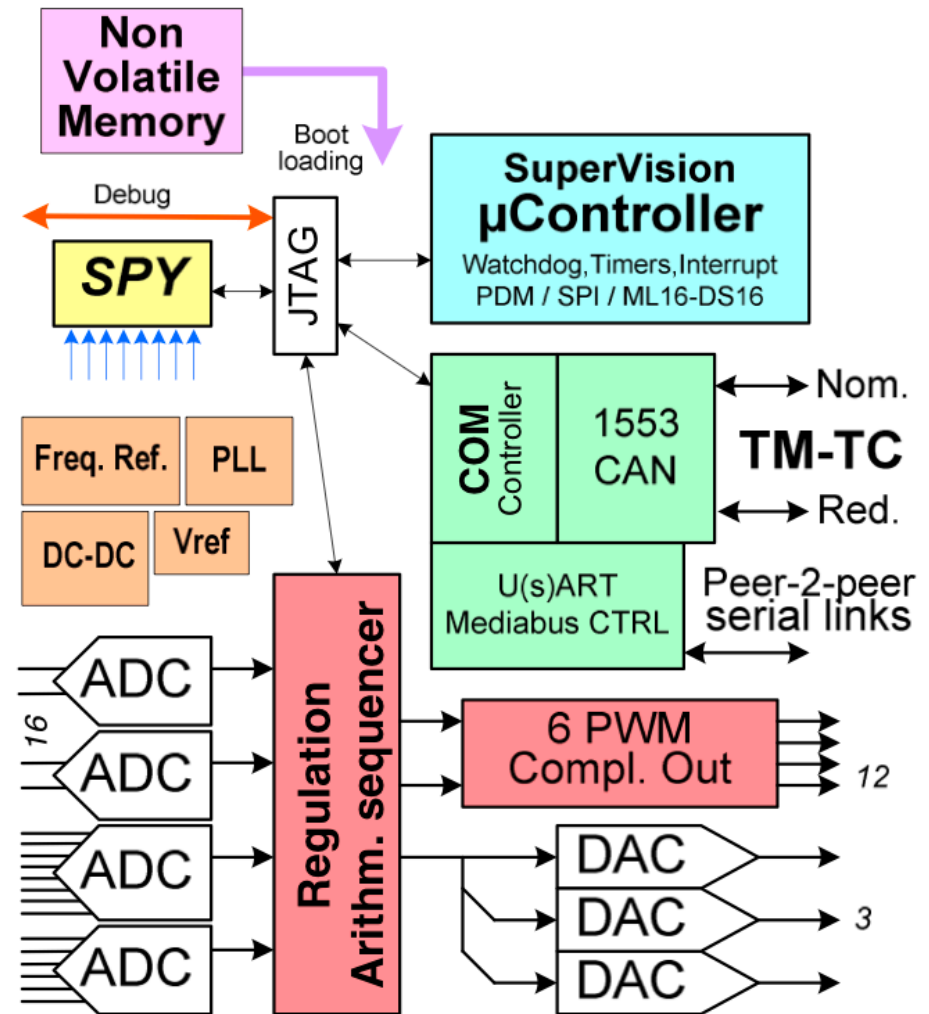
SOC: Digital programmable controller

• Applications:

- Instrument control units
- Digitally controlled power management
- Motor controllers
- Intelligent remote sensor and controllers
- Remote terminal controllers
- Data bus protocol translation (gateway)

• Requirements

- TID 100krad
- SET 60MeV.cm²/mg for e.g. PLL



ADCs

- Core of all ADCs is identical
 - Cyclic pipelined topology
- Extensive input muxing
 - Up to 8 analog single-ended or 4 differential signals
 - Sampling time and channel selection is controllable by MCU
 - On-chip temperature sensor
 - Offset calibration by shorting inputs
 - Sensing amplifier chain
 - Sense very small differential input signals
 - Targeted to measure shunt currents

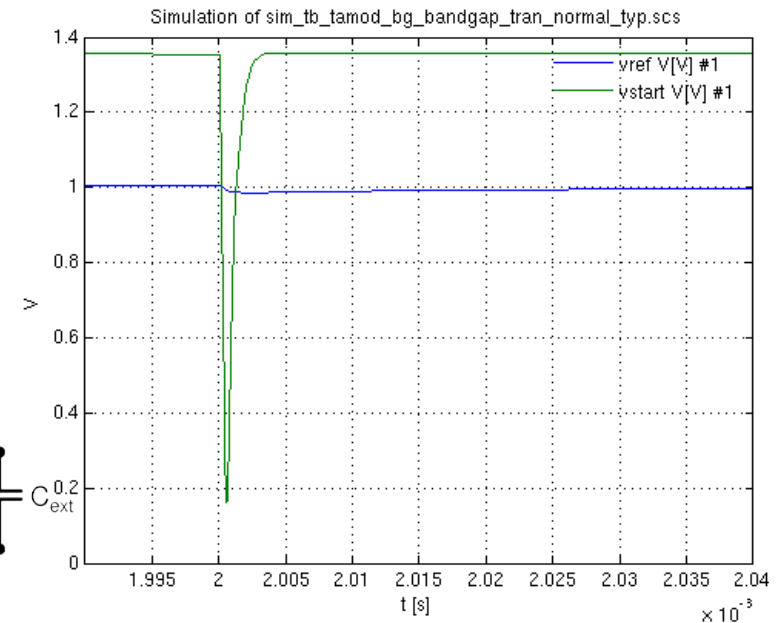
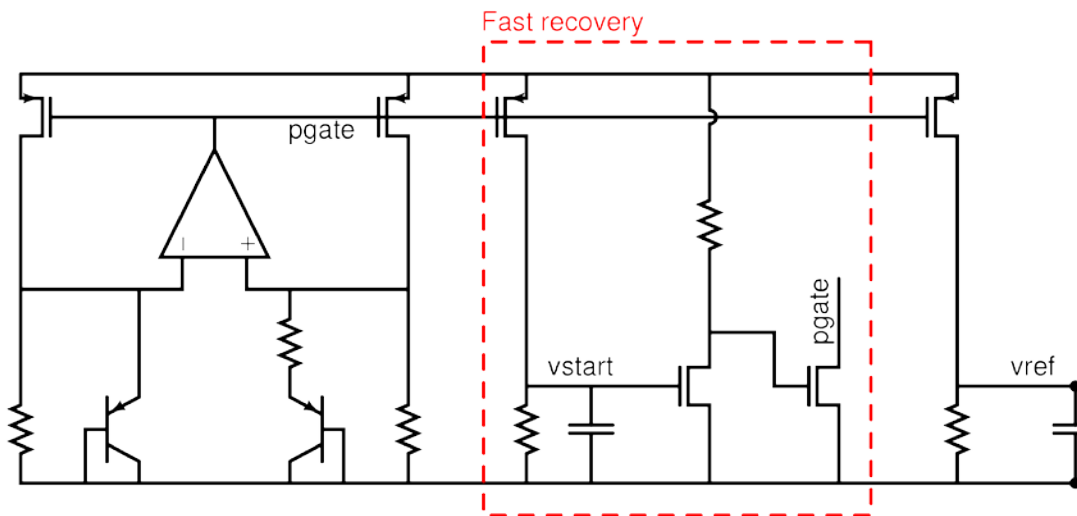
Specification	Value
Number of bits	13
Output data rate	1 MS/s
Input range single-ended	0 – 2.5 V
Input range differential	-1.25 - +1.25 V
INL	6 LSB
DNL	1 LSB
Current consumption of 1 core	6 mA @ 1.8V

Reference voltage of DPC

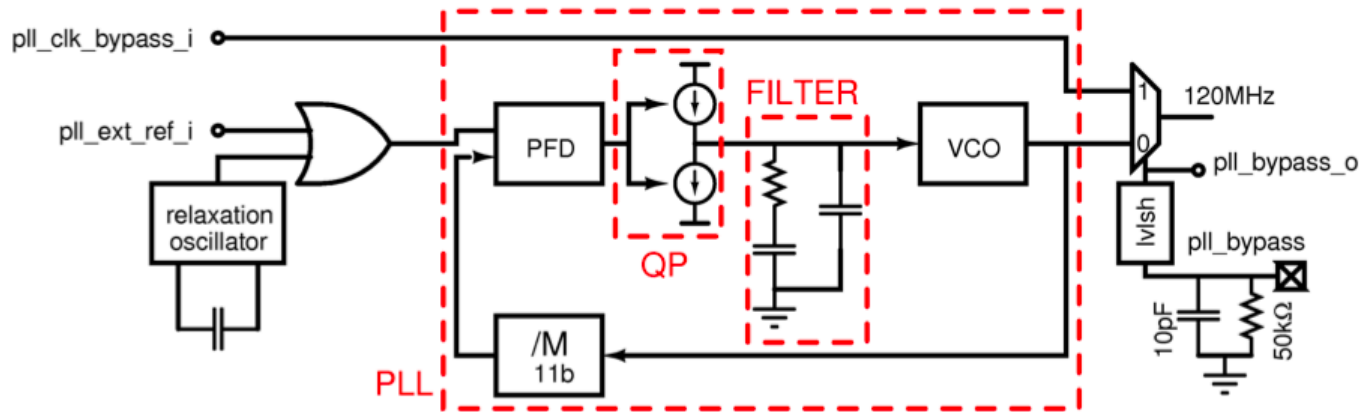
- Bandgap with external buffer capacitor
 - SET sensitivity checked up to $60\text{MeV}\cdot\text{cm}^2/\text{mg}$ on all nodes
- Untrimmed accuracy $< 2\%$
Temperature drift $< 0.6\%$
- Startup circuit
 - Traditional circuit monitors output node of the bandgap.
 - Risk for SET due to e.g. glitch on ENABLE control input of the bandgap
 - Bandgap core will be completely shutdown
 - Output voltage will slowly drop due to large external capacitor
 - Startup circuit will take a long time to react since external capacitor prevents it from being triggered
 - Result: very slow recovery
 - Solution: Replica reference circuit to ensure fast reboot

Reference voltage of DPC

- Internal replica reference voltage for fast recovery
 - ENABLE glitch will immediately effect replica voltage and ensure fast activation of startup circuit
 - Bandgap core recovers very fast
 - Effect on the reference voltage is minimal



PLL



Specification	Value
Relaxation oscillator frequency	100 kHz
PLL output frequency	120 MHz \pm 10% after SET
Cycle-to-cycle jitter (over 480 cycles)	14ps

- PLL must ensure reliable operation under SET of digital cores
 - No clock glitches
 - No additional/skipped clock cycles

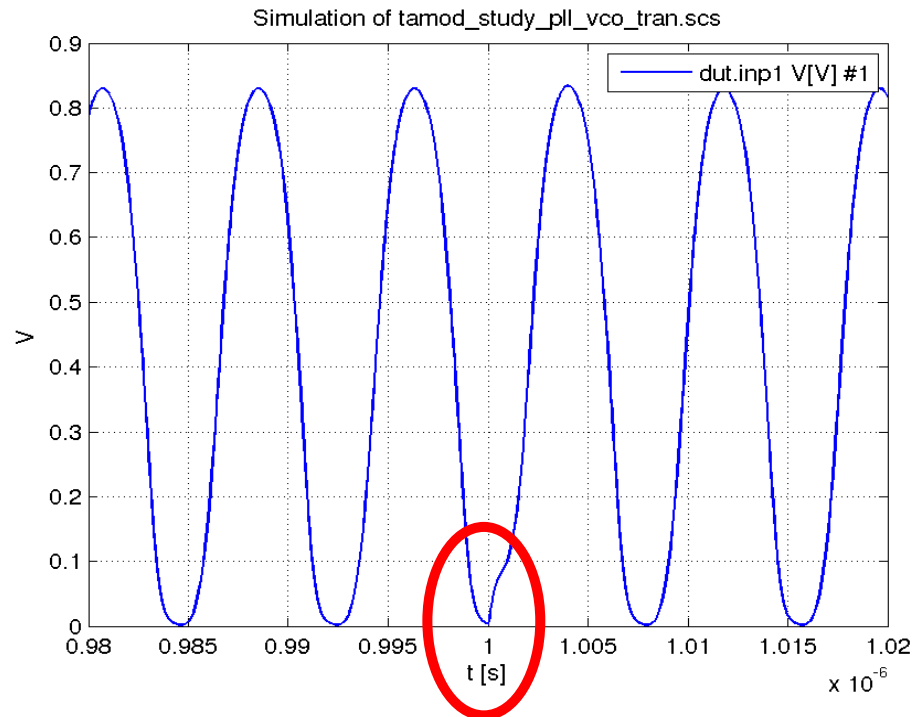
PLL

- Relaxation oscillator

- External R and C for excellent stability and temperature drift
- Triplicated comparator for SET
- Special topology to combine low jitter and low T drift.
- T drift is dominated by external components

- VCO

- VCO is based on derivative of Manassis delay cell
- SET sensitivity reduced by increased current levels and capacitance values
- Simulation plot shows impact of SET strike in internal node of the VCO



Design flow for SET

- SET of 60 MeV.cm²/mg
 - inject double exponential current with total charge of 1.2pC
- Flow procedure for building-block SET simulations
 1. Typical conditions: inject in every node to produce short list of sensitive nodes
 2. SET simulations for all sensitive nodes over PVT.
Adapt design if needed by
 - Increasing current levels
 - Add buffer caps
 - Topology changes
 3. Re-inject all nodes in worst-case corners
- Clock signals: vary also injection time relative to clock period
- Top level: check e.g. if SET on bandgap does not influence PLL
- Fully automated flow integrated into our MATLAB driven design environment

Design flow for TID

- Vth shifts: monitor $V_{DS} - V_{DS,SAT}$ of every device over PVT corners to ensure that sufficient margin is present to accommodate Vth shifts
- Ensure that bias conditions of matching structure are identical in all operation modes
- Extra DRC rules to check for proper P+ guard-ring inbetween N+ regions with DARE ADK
- Analog block with highest matching sensitivities use 1.8V devices
- 3.3V parts use ELT devices for NMOS.

Top level verification: wreal modeling

- Top-down bottom-up design approach
 - Good models are essential to provide good coverage of all operation modes for a mixed-signal ASIC
- Modeling approach: wreal
 - Verilog-AMS with wreal data types for analog parts
 - No analog parts of verilog-AMS language are used in the models
 - Wreal discipline is continuous in amplitude and discrete in time
 - Event-based simulation in digital simulator → fast
- Key advantages
 - Identical models are used by digital team and analog team
 - Early start of top-level functional verifications
 - Top-level mixed-signal simulations: full flexibility in trade-off between simulation accuracy, coverage and simulation speed
 - Digital part: verilog
 - Analog part: extracted layout / schematic / model

Questions?

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