Business from technology

AMICSA 2012

Integrated SAR Receiver/Converter for L, C and X bands

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The Team

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Outline

- Requirements
- Chip design
- Verification
- Compliance statement
- Outlook for further improvements
- Conclusion

Requirements

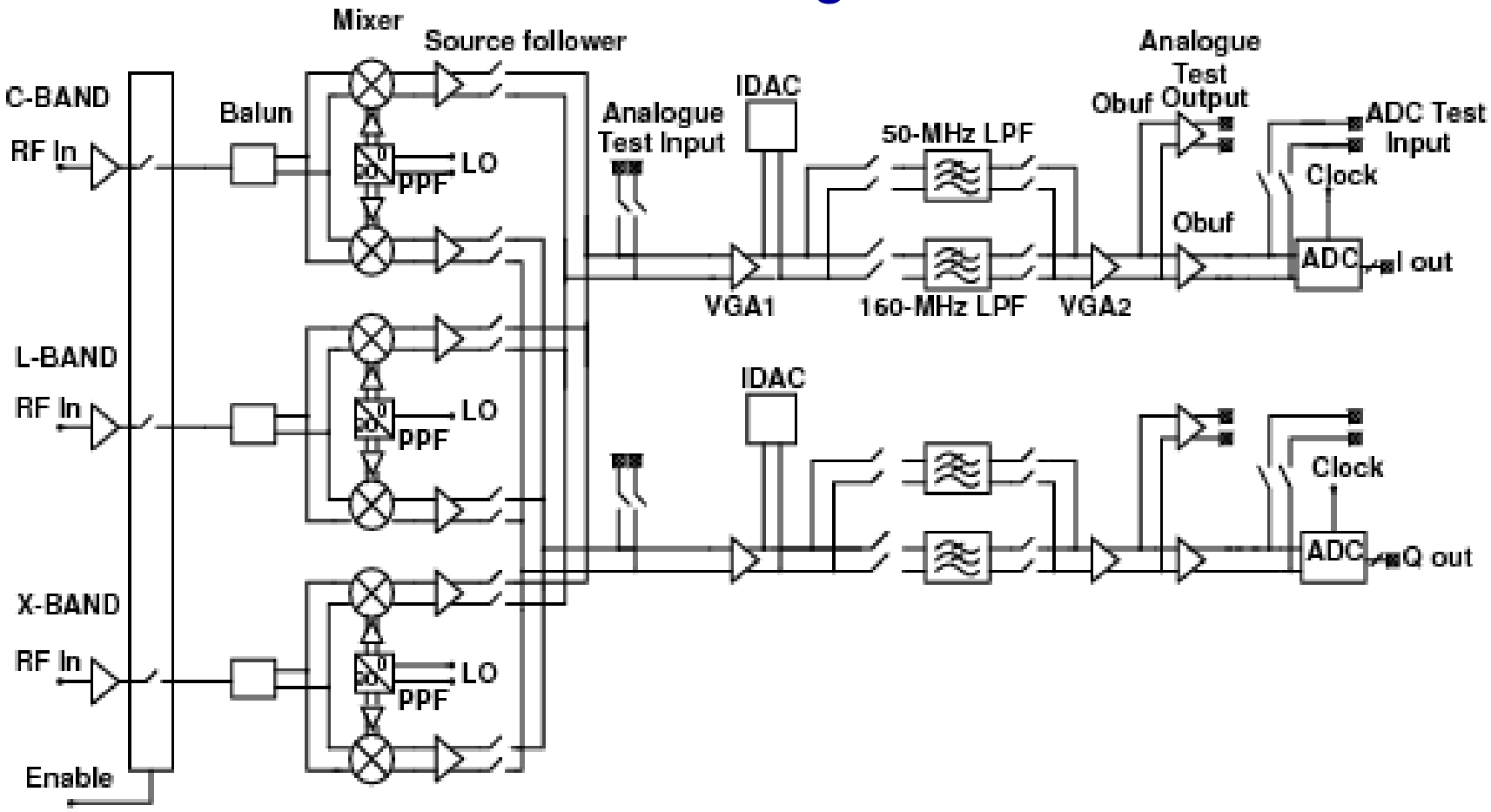
- Final specifications

REQ-ID	Name	Original ESA specification	
A.2.1.1 General Functional Requirements			
2.1.1-1	**Bands**	C,L,X, two BWs 320 and 100 MHz	
2.1.1-2	**ADC scalability**	8 to 5 bit	
2.1.2-3	**Digital output**	I-Q format	
2.1.2-8	**LO power**	< 7 dBm	
2.1.2-9	**NF within Bandwidth**	< 10 dB	
2.1.2-11	**Gain Flatness vs. Bandwidth**	±1.5 dB Goal ±0.5 dB	
2.1.2-12	**Phase linearity vs. Bandwidth**	±5 deg (TBC)	
2.1.2-18	**IMD**	-60 dBc, at -15 dBFS, 8 bits	
2.1.2-22	**Max power consumption**	900 mW	
2.1.2-24	**I/Q gain balance**	±0.5 dB	
2.1.2-25	**I/Q phase balance**	±5 deg	
2.1.2-26	**Alias signal suppression**	>30 dB	

Chip Design

- Chip design
- - block diagram
- - circuit highlights
- - chip interfaces

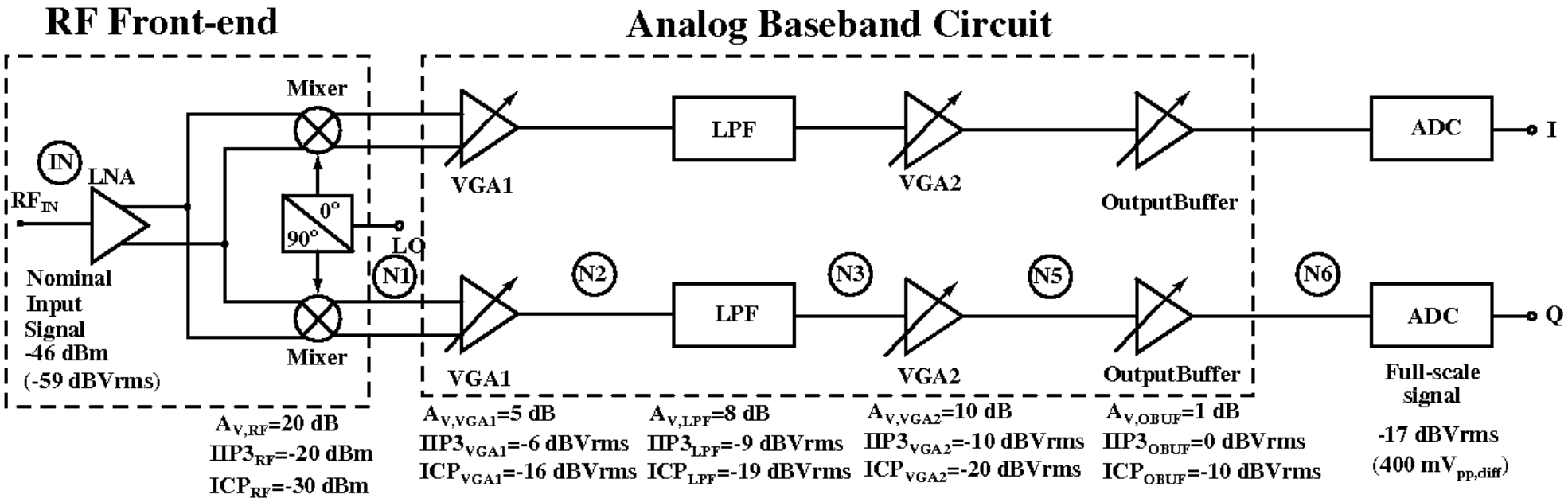
Block diagram



Block diagram of the circuit. IDAC = current-steering D/A converter.

LNAs & filters external

Gain Allocation

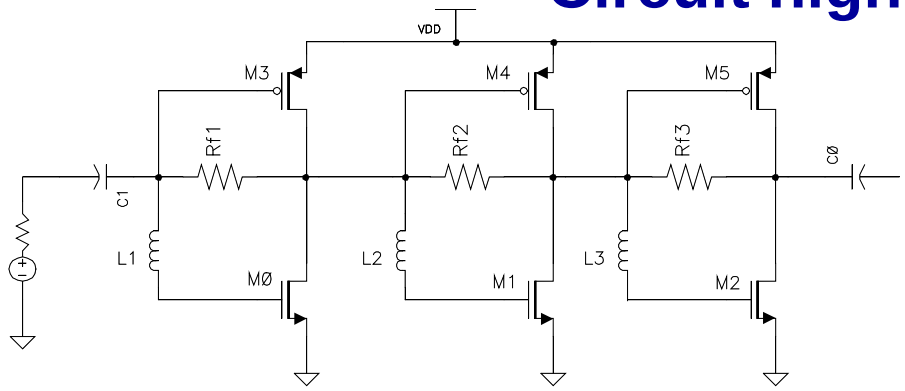


With -46 dBm input signal, needed gain for full-scale signal at ADC input is 42 dB.

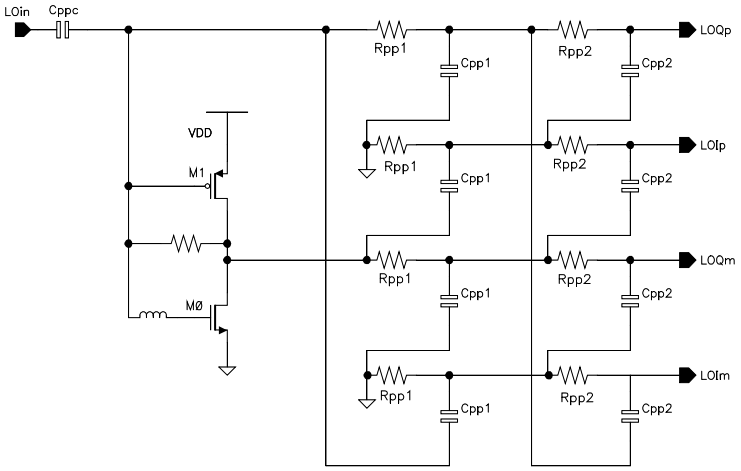
Circuit highlights, RF

- The RF front end consists of:
  - an amplifier,
  - an active balun,
  - two Gilbert cell mixers
  - a passive polyphase filter for the LO signal
  - two controlled attenuators in the signal path.
    - the first is after the amplifier and
    - the second is after the mixers.

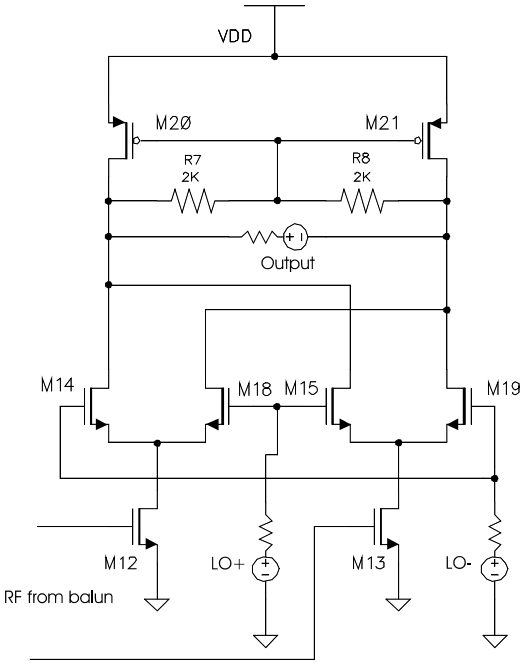
Circuit highlights, RF



Wideband amplifier schematic C and X band; L band similar but without the peaking inductors L1-L3



Two-stage polyphase filter schematic L-band; C and X band have differential input.

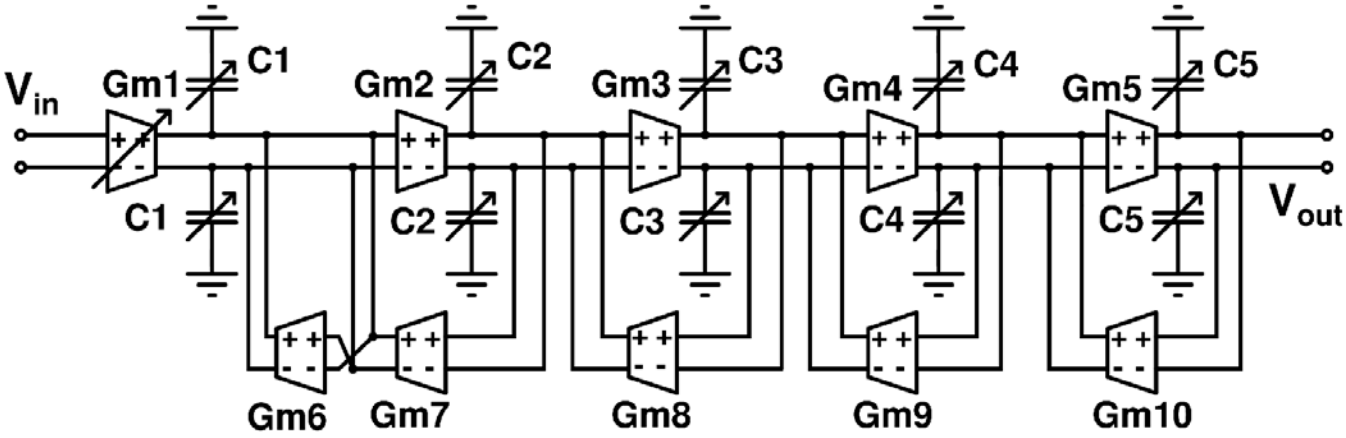


Mixer schematic

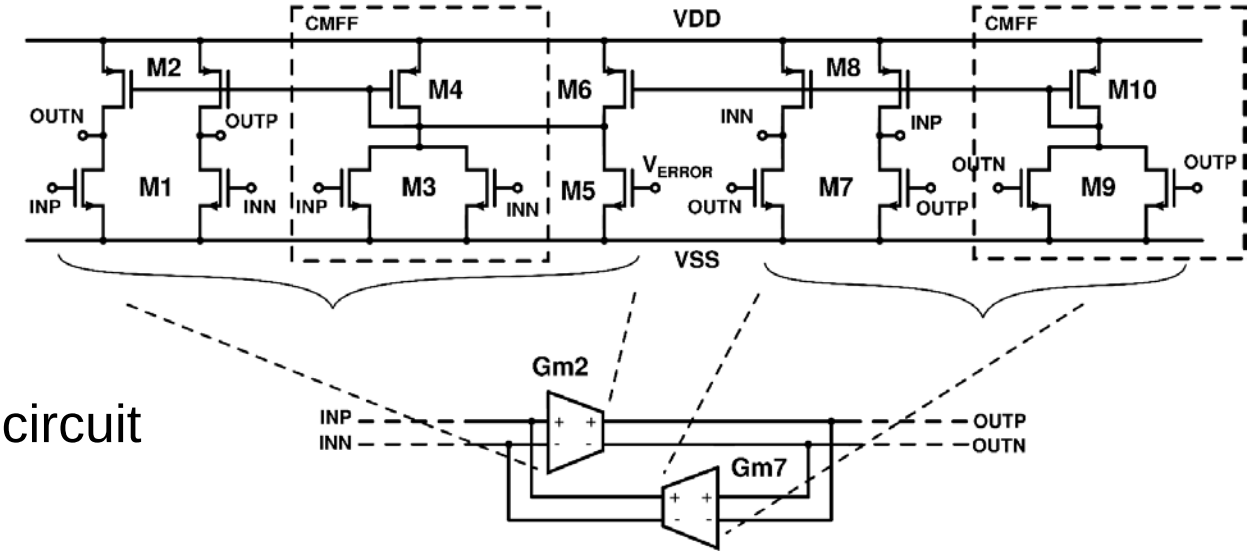
Circuit highlights, BB

- The baseband block consists of:
  - a source follower designed to drive a large parasitic capacitive load,
  - two VGAs (VGA 1 and VGA2),
  - An IDAC to compensate dc offset
  - a 5th-order 160-MHz and 5th-order 50-MHz low-pass filter,
  - an output buffer designed to drive the following 8-bit ADC
  - an analogue test output

Circuit highlights, BB



Fifth-order gm-C low-pass filter

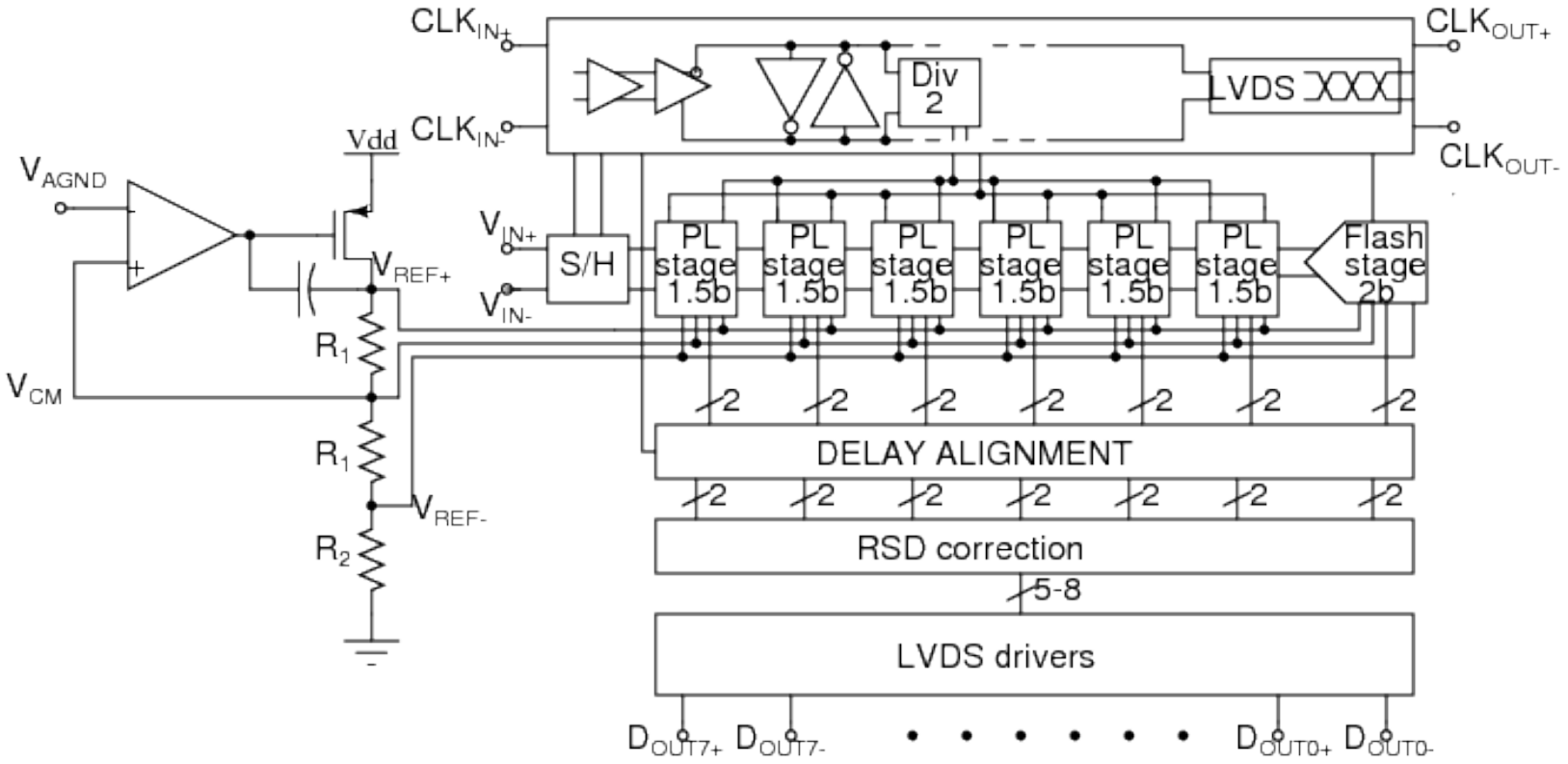


Transconductor circuit

Circuit highlights, ADC

- The analogue-to-digital converter (ADC) circuit consists of:
  - a sample and hold (SH) front-end,
  - six switched capacitor (SC) double-sampling 1.5-bit pipeline stages,
  - and a 2-bit flash back-end stage

Circuit highlights, ADC

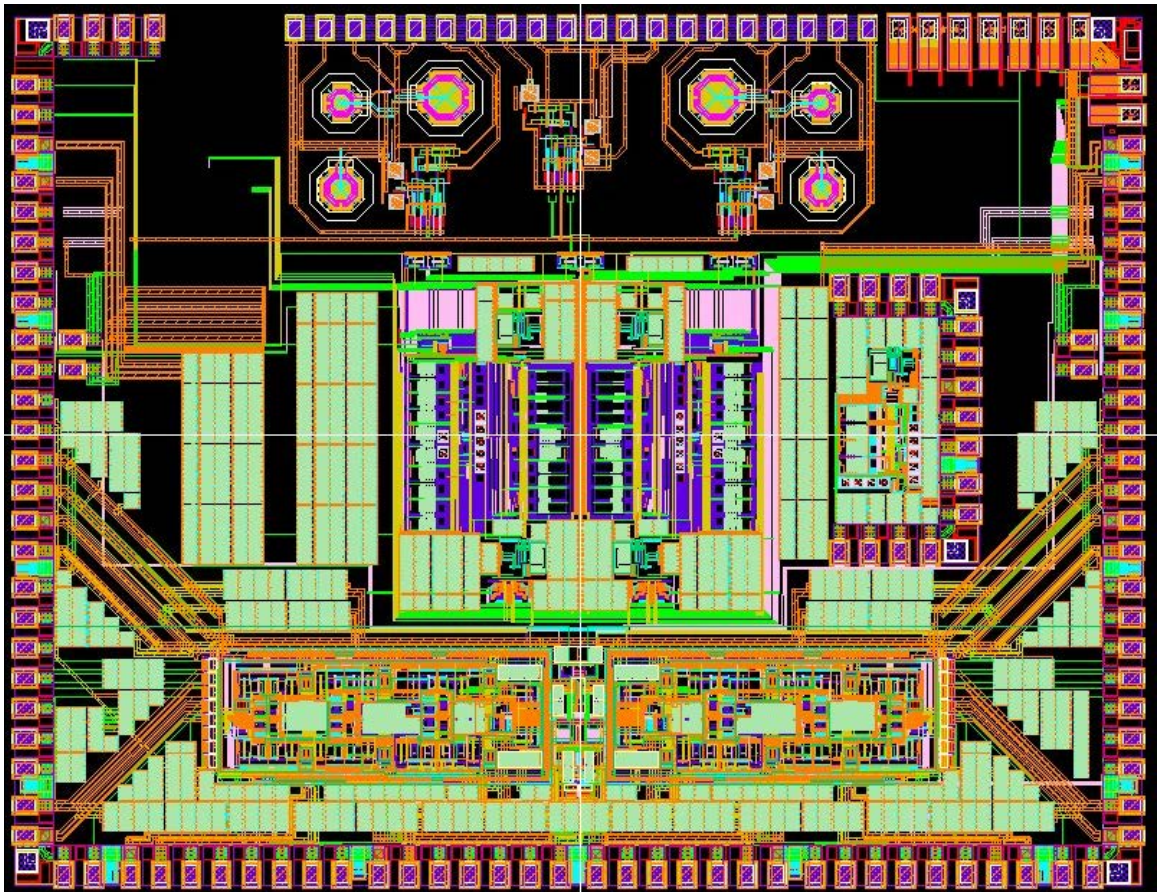


The ADC block diagram including the on-chip reference voltage buffer

Chip interfaces

rf inputs: C L X

LVDS outputs



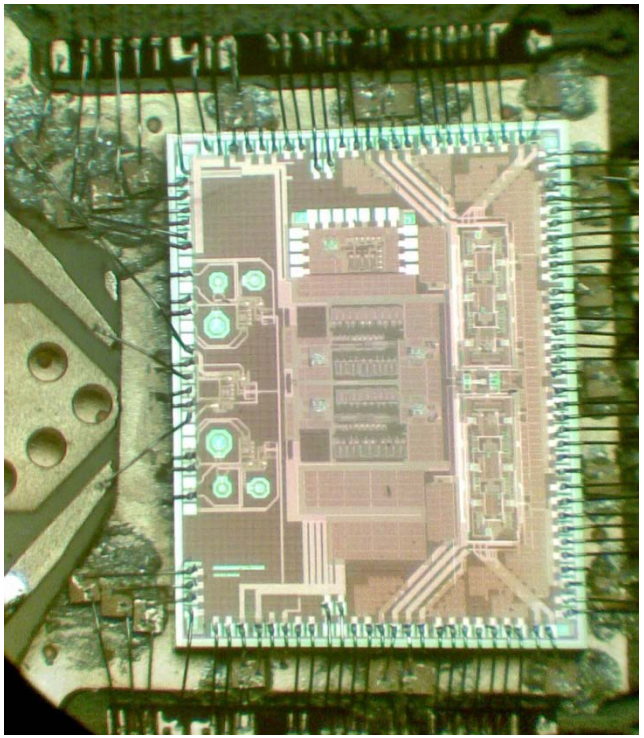
LVDS outputs

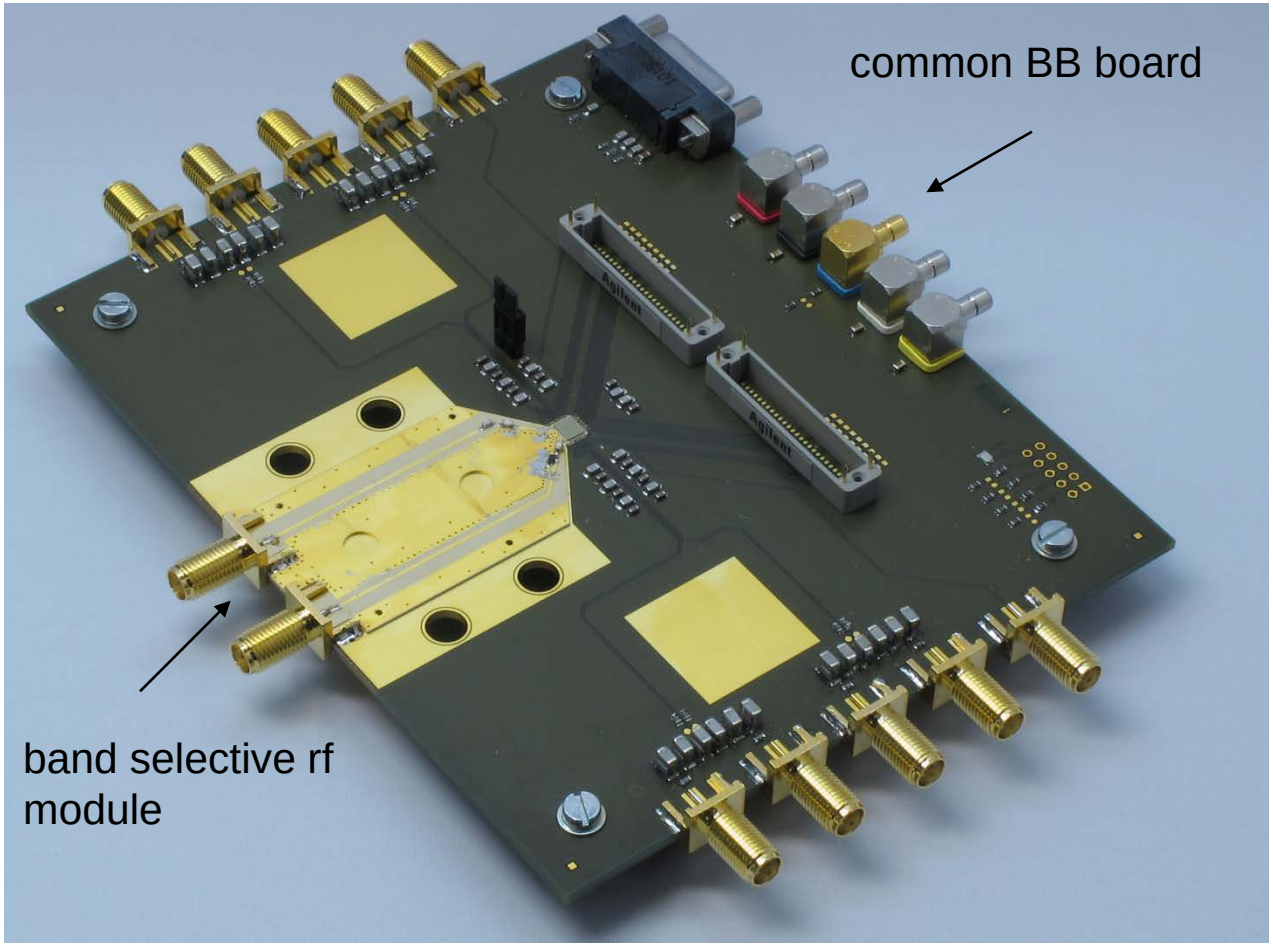
LVDS outputs

Verification

- Verification:
- - test board
- - test results BB
- - test results ADC
- - test results C-band
- - test results L-band
- - test results X-band

Test board





LO-leakage

During the board design serious LO-leakage problem arose.

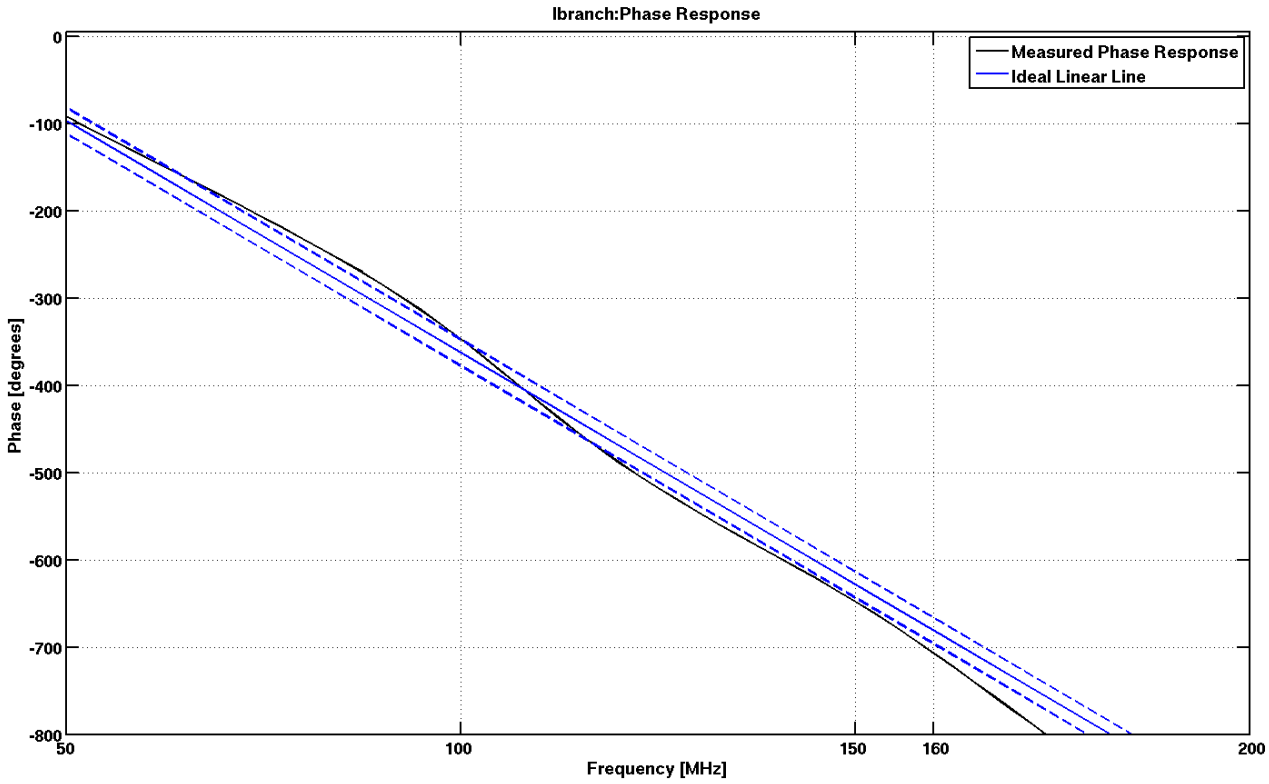
- L-band LO-RF isolation -36.5 dB (single ended)
- C-band LO-RF isolation -35 dB (differential)
- X-band LO-RF isolation -32 dB (differential)

Consequences of the leakage

- High dc-offset due to the ”phase detector behaviour” in mixers
  - Could not be totally compensated in all temperatures
- Possible compression of RF-amplifier

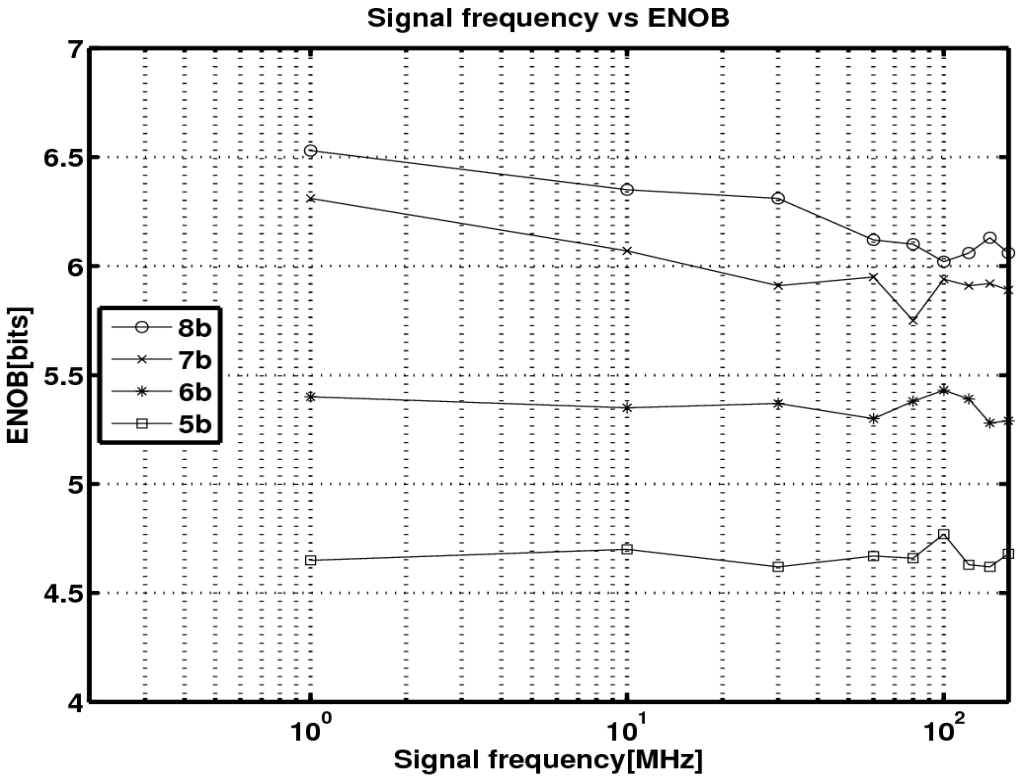
It turned out that fairly extensive testing of both L- and C-band systems could, anyway, be carried out.

Test results BB



Phase linearity of the 160MHz filter with ± 15 degree pipe

Test results ADC



Summary of the ADC measurements

Mode	P[mW] (1 ADC)	DNL[LSB]	INL[LSB]	ENOB[bits]	ERBW[MHz]
8	100	0.38	0.577	6.53	200
7	84	0.31	0.46	6.30	200
6	66	0.33	0.374	5.40	1000
5	50	0.35	0.32	4.70	>1000

Test results

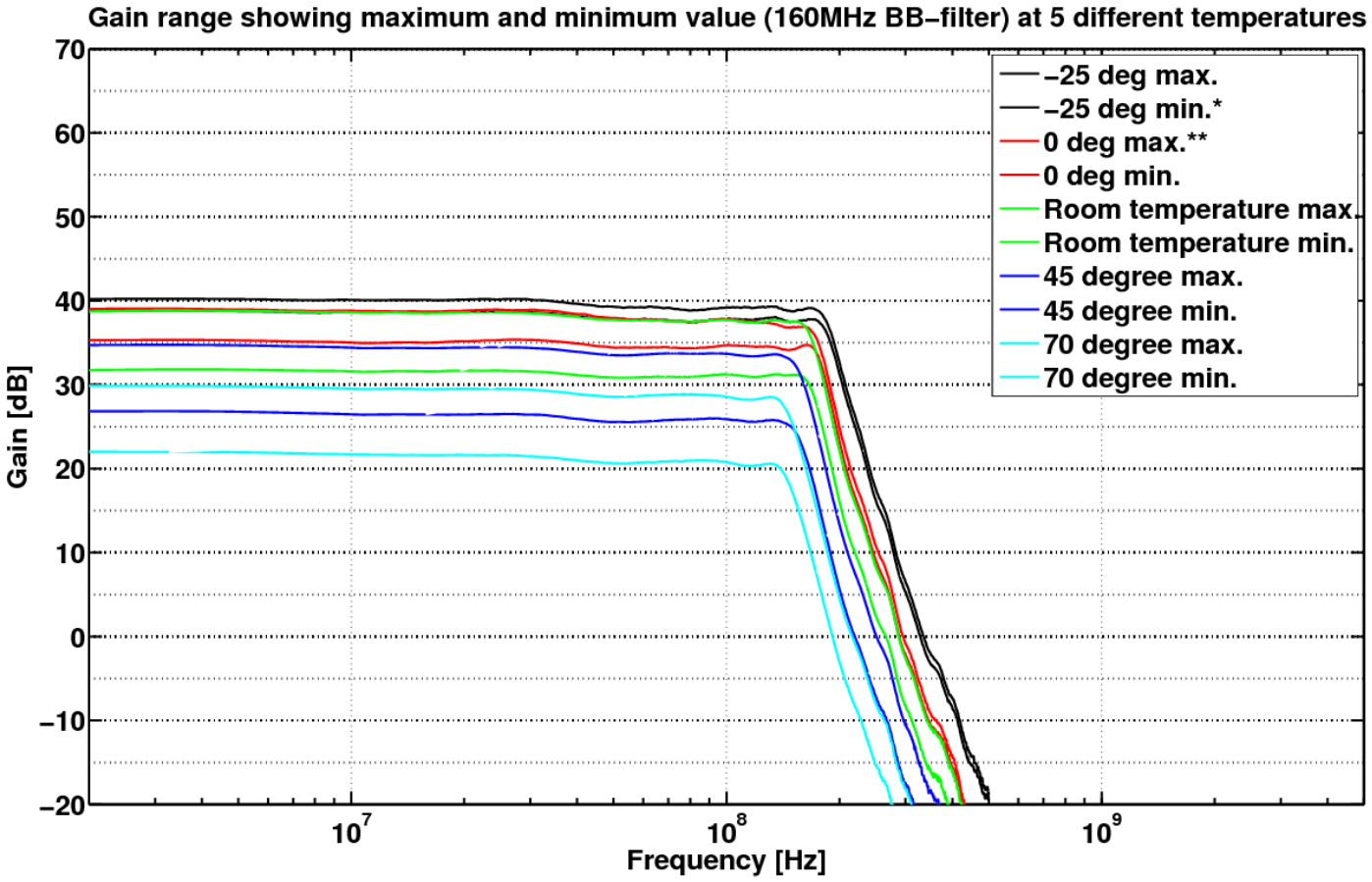
parameter	320 MHz	100 MHz	comments
Power consumption	≈800 mW	≈650 mW	ADC 8-bit mode
Alias signal suppression	>30 dB	>30 dB	
Dynamic range	38 dB	43 dB	

Common parameters

Test results C-band-Introduction

- The measurement were done in 5 different temperatures (-25 deg, 0 deg, 22 deg,
- 45 deg and 70 deg).
- All the measurements have been performed at the analog test output, Q branch.
- The method was to use the same tuning setting as in room temperature (22 deg) in all different temperatures. If the setting gave erroneous results, than tuning is done to get correct results.
- In IQ imbalance measurement, the common, main gain tuning (VGA1) for both of the branches are kept the same in all temperatures. Only the fine gain tuning and the DC-offset compensation tuning was done.
- LO-level 5.5 dBm

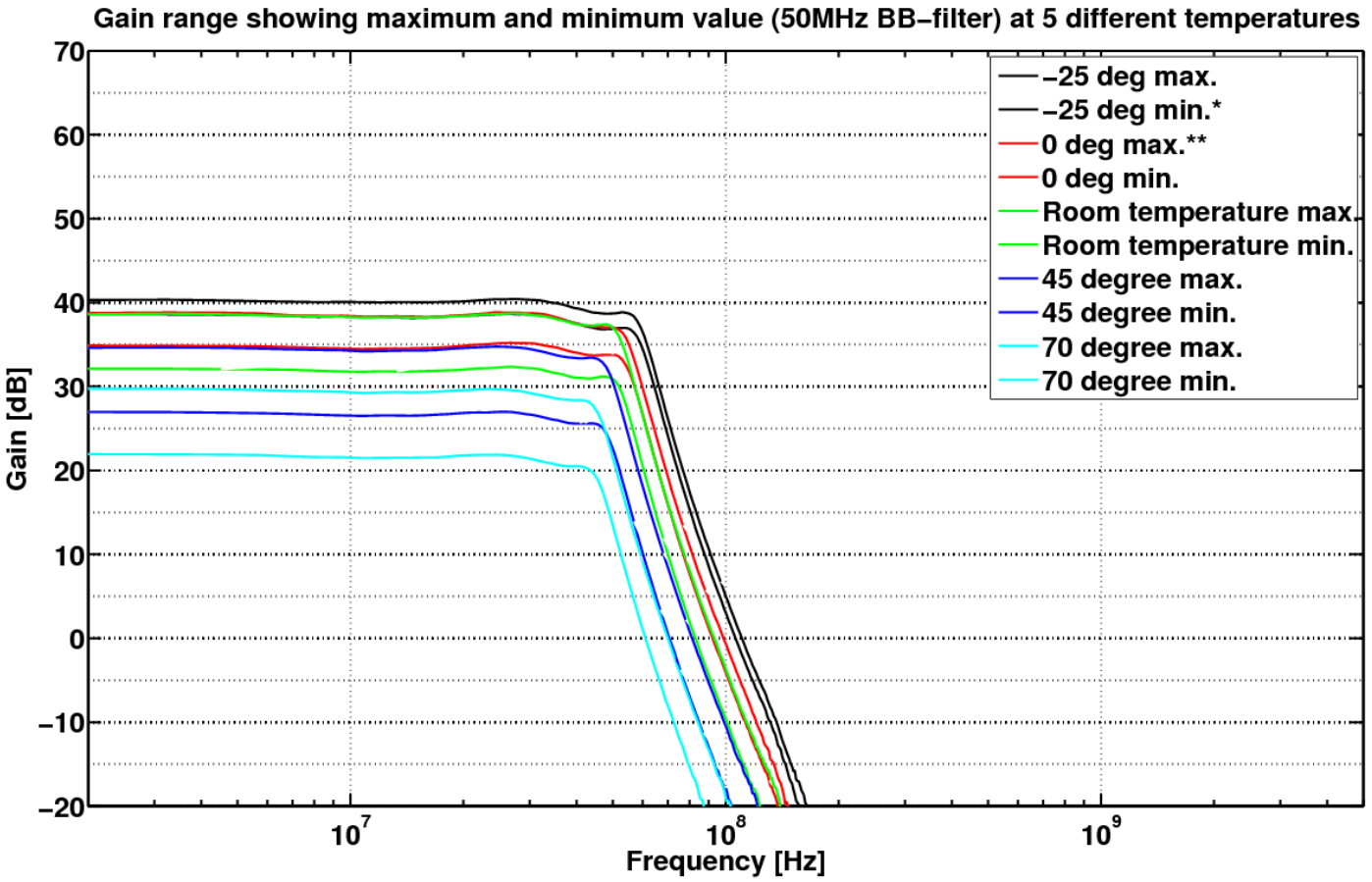
Test results C-band



* The same setting as nominal gain at -25 degree C

** The same setting as nominal gain at 0 degree C

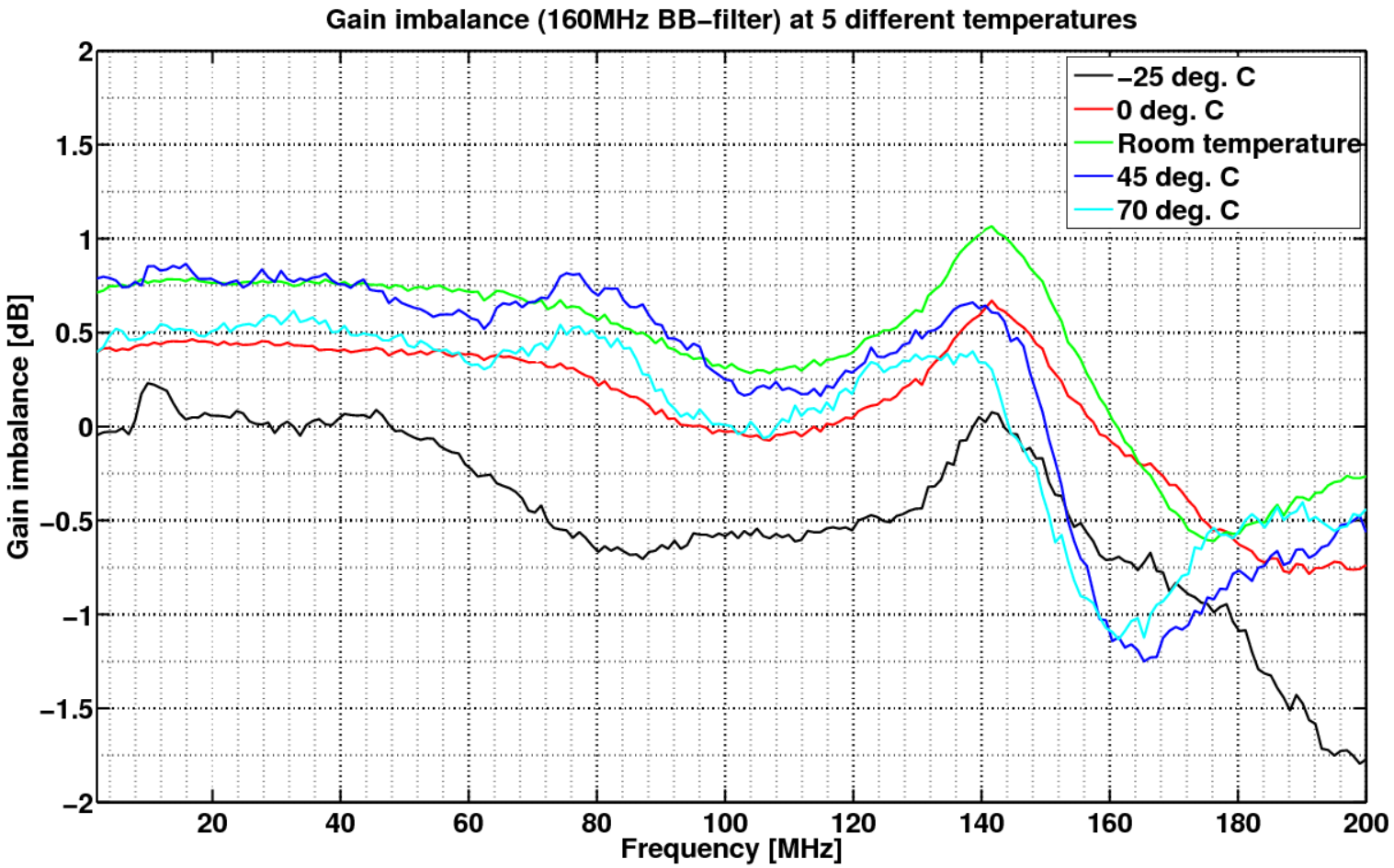
Test results C-band



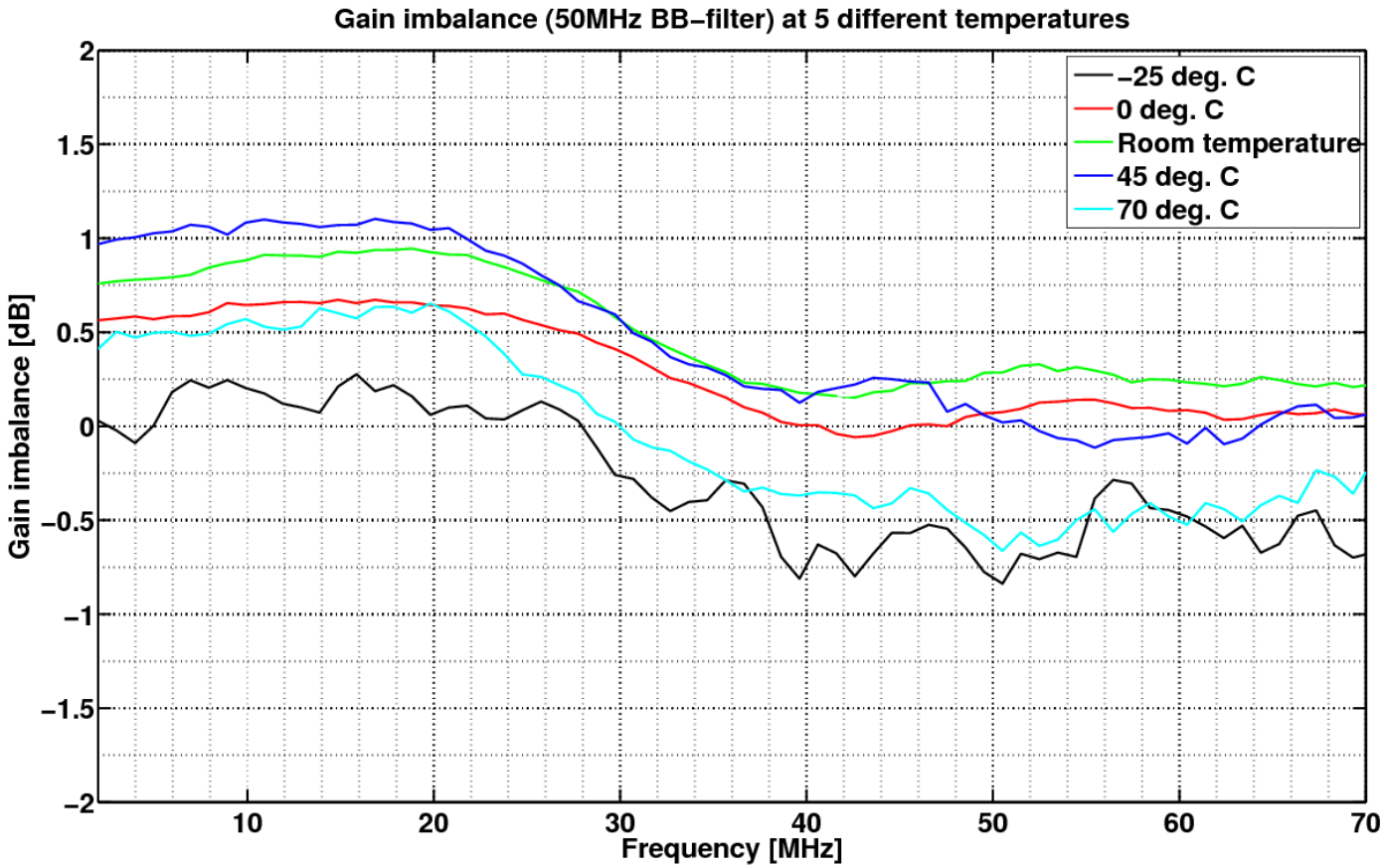
* The same setting as nominal gain at -25 degree C

** The same setting as nominal gain at 0 degree C

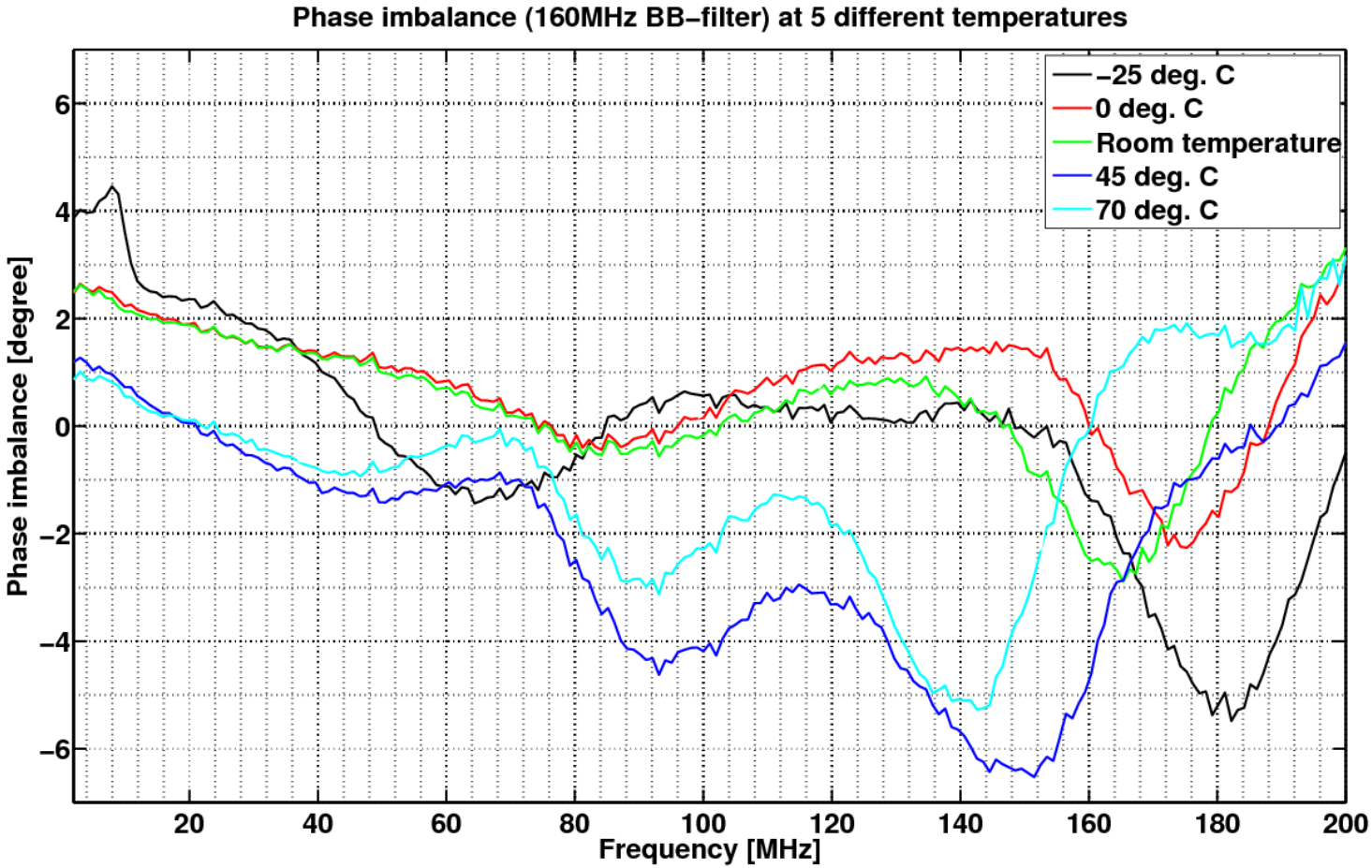
Test results C-band



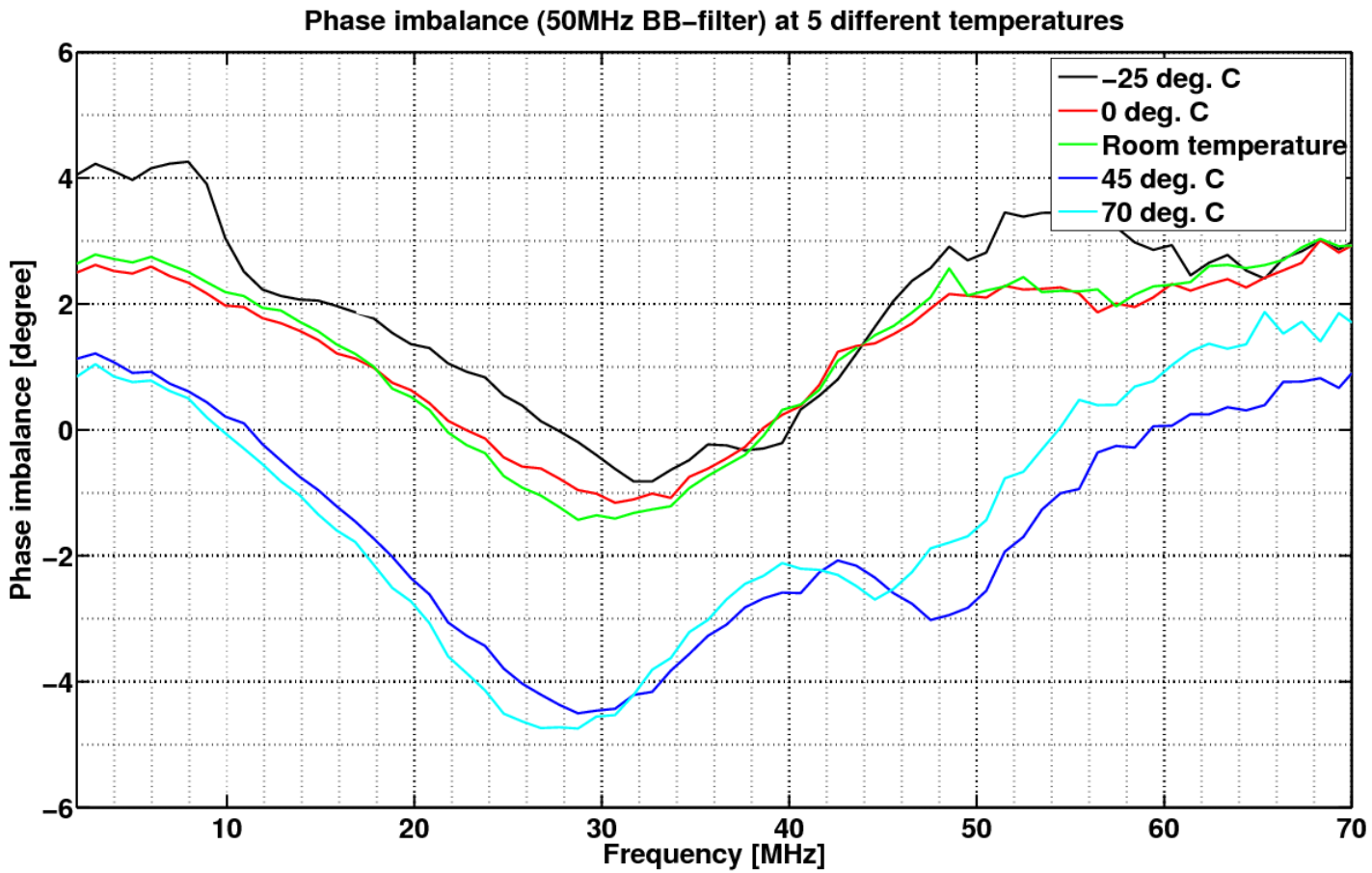
Test results C-band



Test results C-band



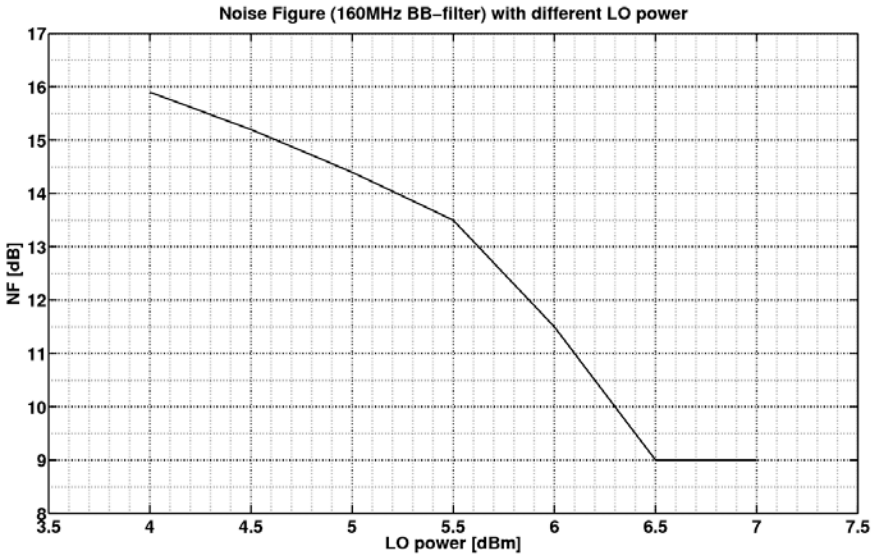
Test results C-band

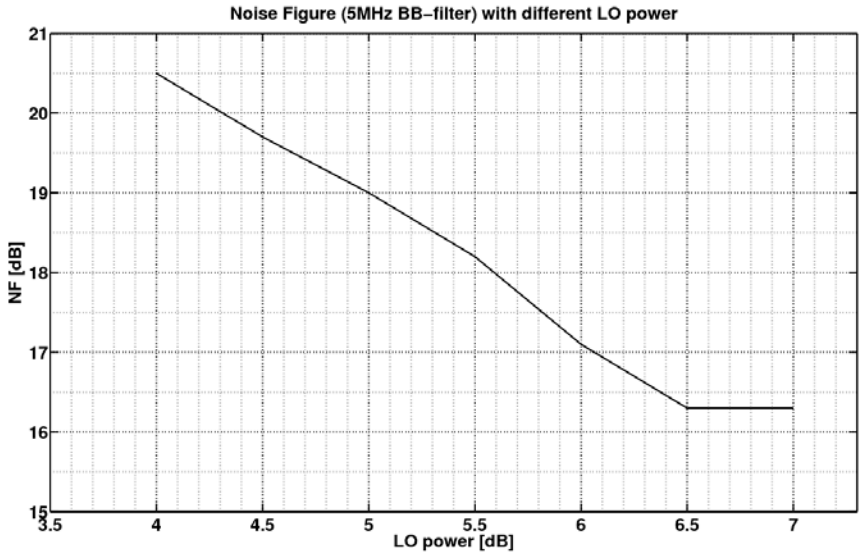


Noise Figure

The maximum LO-level is about 6.5 dBm due to the leakage, nominal in measurements 5.5 dBm.

	L band		C band		X band	
	predicted	measured	predicted	measured	predicted	measured
320 MHz	10 dB	14 dB	11 dB	9.0 dB	17 dB	
100 MHz	15 dB	15 dB	15 dB	16.2 dB	23 dB	



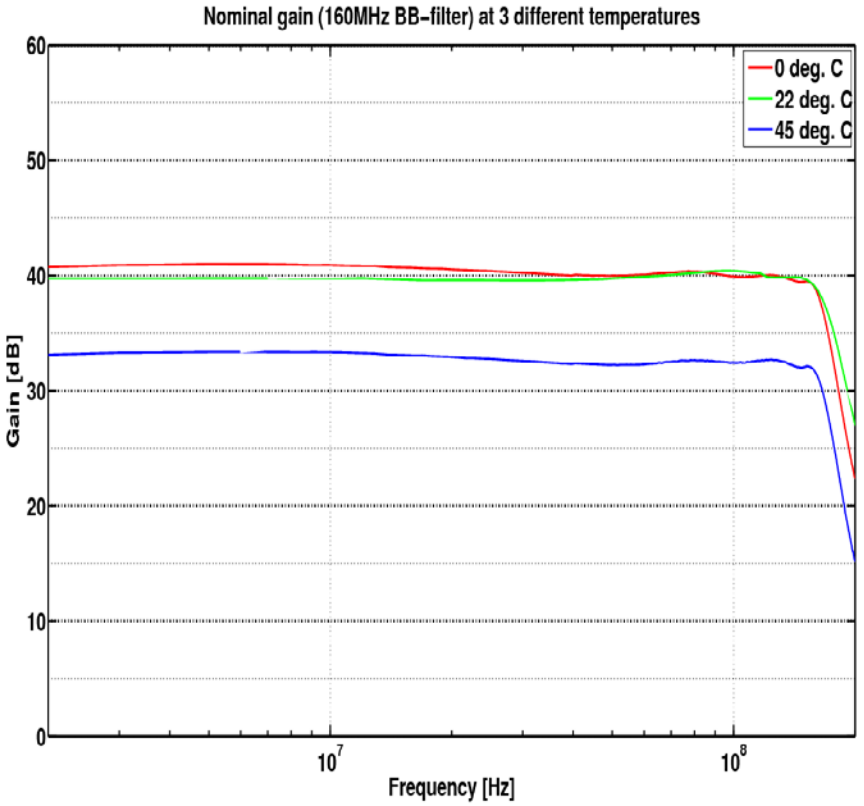


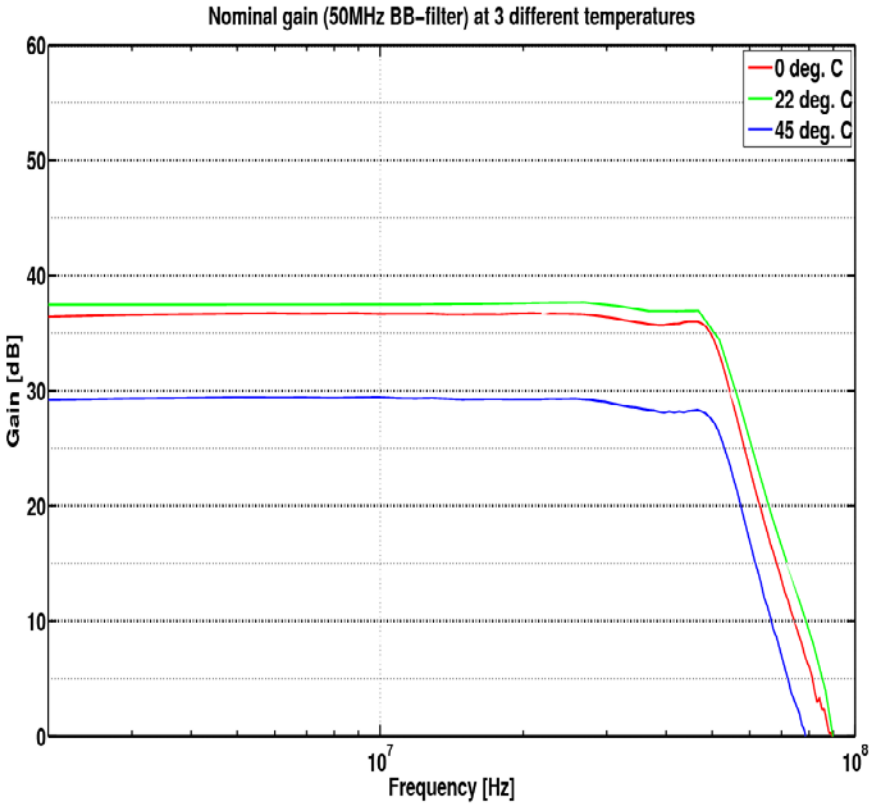
Noise Figure vs. LO-level C-band

Test results L-band-Introduction

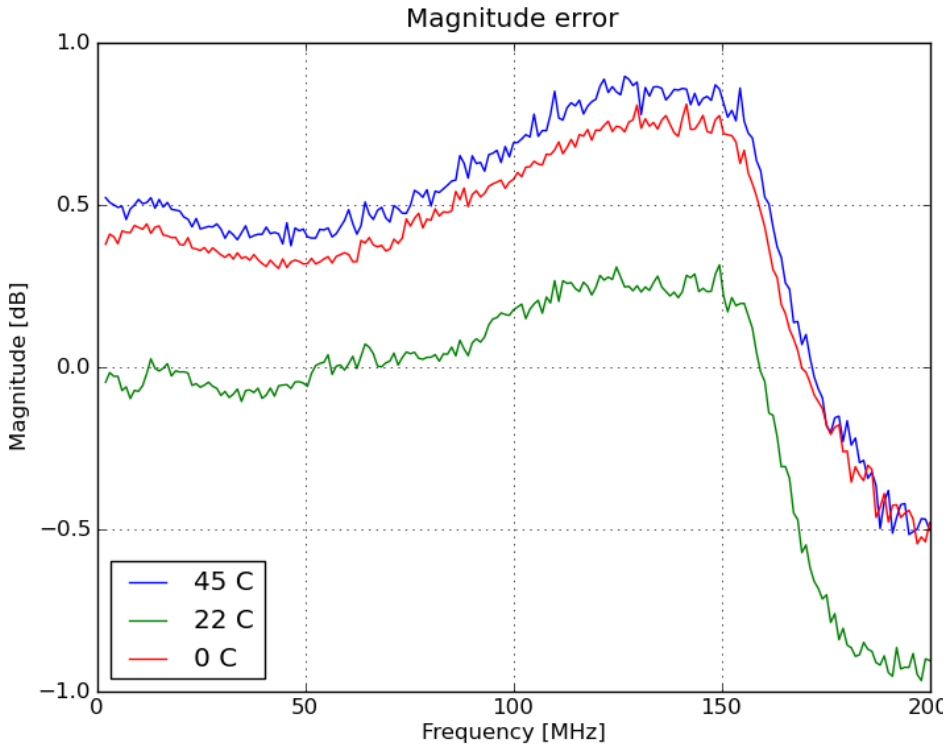
•The measurement were done in 3 different temperatures (0 deg, 22 deg and 45 deg).
• All the measurements have been performed at the ADC test input, Q branch.
• We tried to find the best chip parameter setting in every different temperatures and performed the measurements.
• For IQ imbalance measurement, the optimal gain in different temperatures for different filter bandwidth are used respectively.
LO-level 5.5 dBm

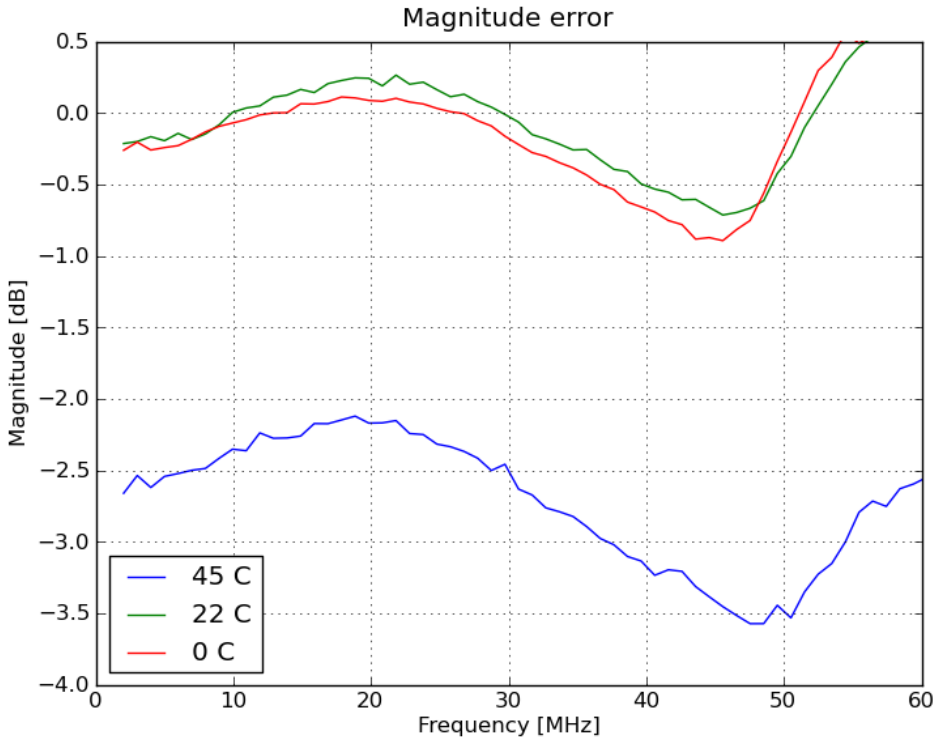
Test results L-band



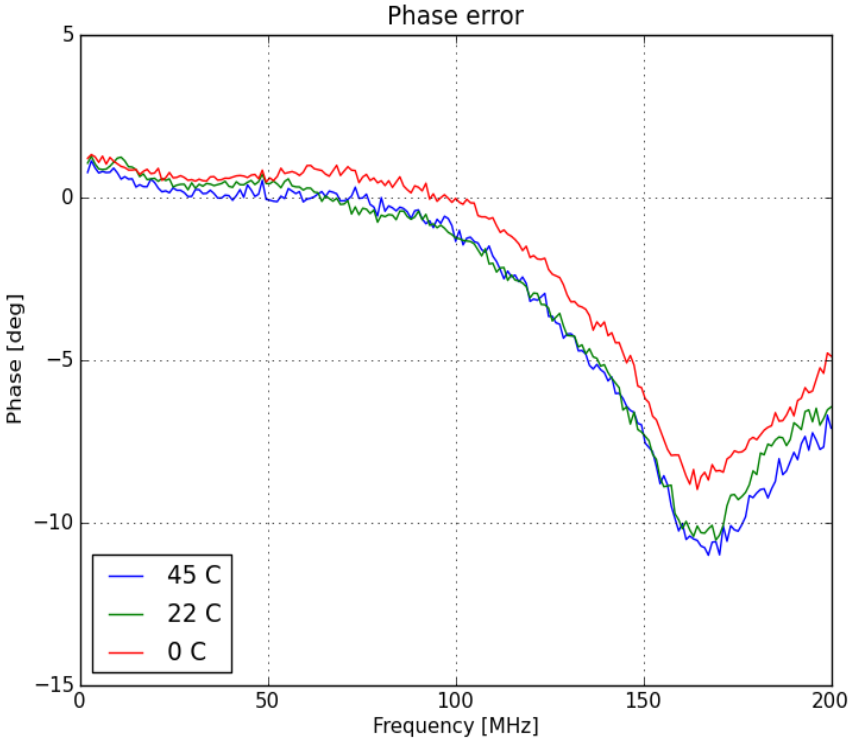


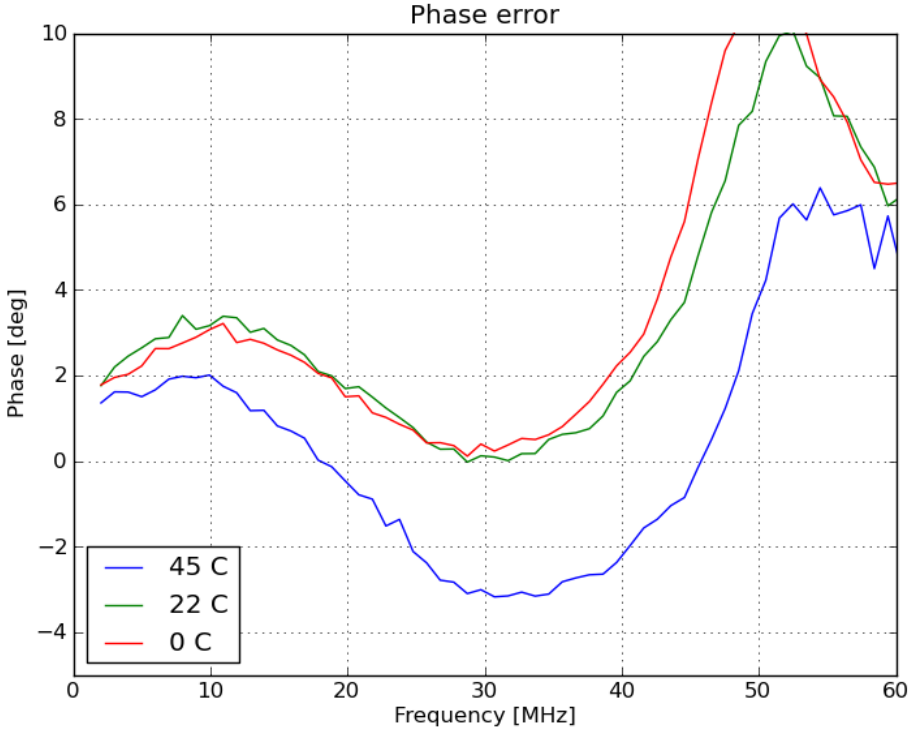
Test results L-band





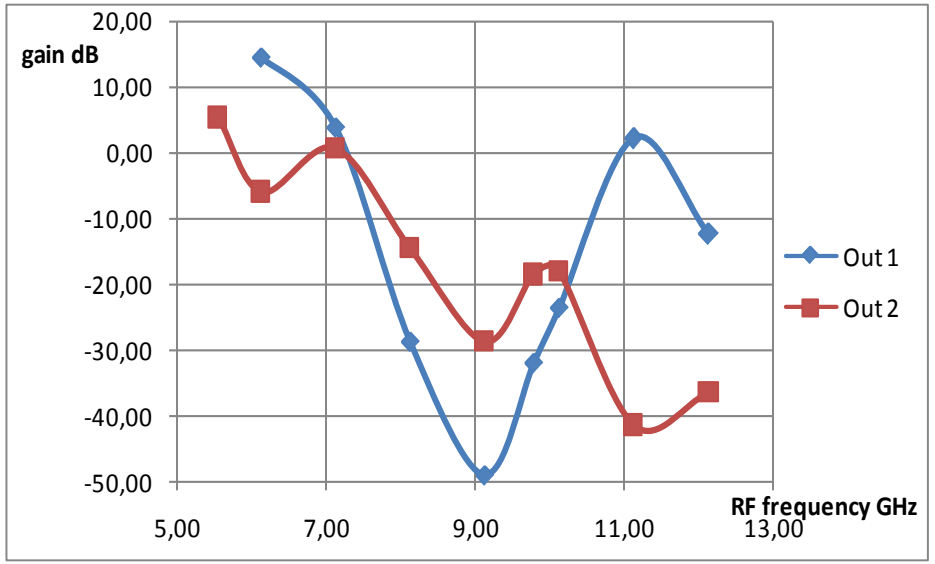
Test results L-band



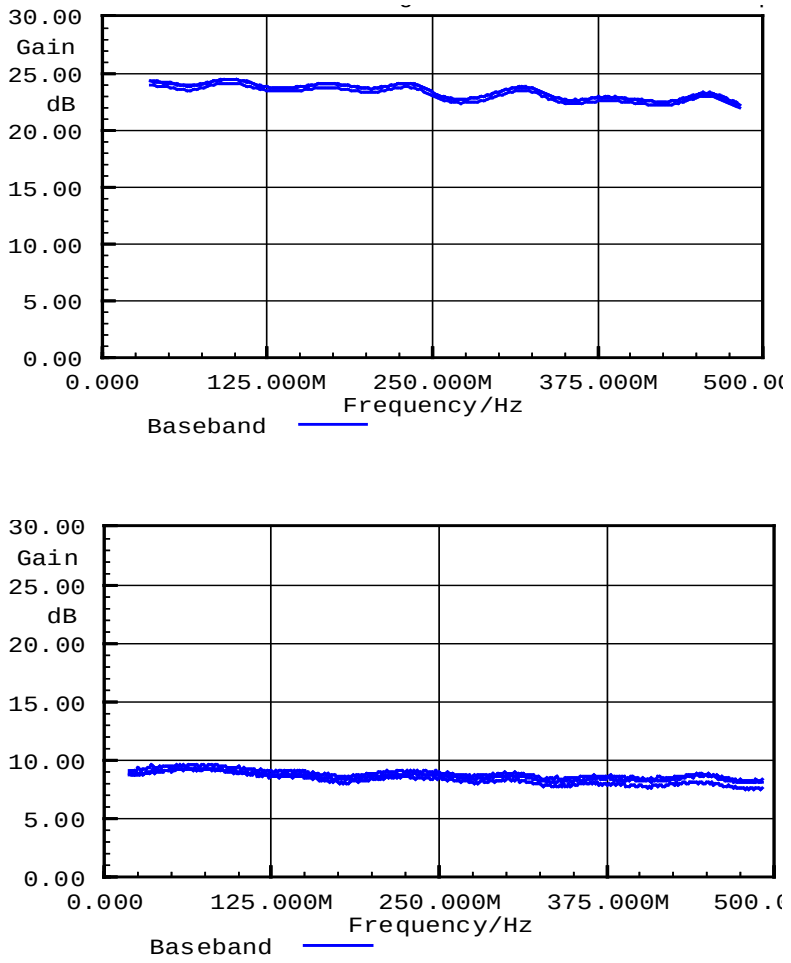


test results X-band

- First run X-band gain only 9 dB
  - Some improvements done, but
- In the integrated version gain collapsed



Wide band measurement of the total gain. The circuit was matched to X-band. Matched L- and C-band total gains were in the order of 40 dB. Out1 is the initial test board result and Out 2 after re-tuning the matching.



First run C and X-band conversion gain

Summary of performance

Name	Final ESA specifications	Compliance (over the temperature range unless otherwise stated)
LO power	< 7 dBm	< 6.5 dBm, before compression.
NF within Bandwidth	< 10 dB	L-b 320 MHz ≤ 11 dB; 100 MHz ≤ 15 dB ≤ 22°C; LO 5.5 dBm C-band 320 MHz 9 dB at T 22°C, LO 6.5 dBm C-b 320 MHz ≤ 13.5 dB; 100 MHz ≤ 18 dB ≤ 22°C; LO 5.5 dBm
Gain Flatness vs. Bandwidth	±1.5 dB Goal ±0.5 dB	C-band 2.3 dB worst case L-band 2.0 dB worst case
Phase linearity vs. BW	±5 deg (TBC)	±15 deg
DNL	±0.5 LSB	Yes, ±0.38 LSB
INL	±0.5 LSB	±0.58 LSB
IMD	-60 dBc, at -15 dBFS, 8 bits	-50 dBc, at -15 dBFS, 8 bits
Max power consumption	900 mW	max 800 mW (8 bits, 320 MHz) min 500 mW (5bits, 100 MHz)
I/Q gain balance	±0.5 dB	C-band ±1.1 dB, L-band ±0.8 dB
I/Q phase balance	±5 deg	C-band ±5 deg, L-band ±7 deg (both±2.5 deg to 280/80 MHz)
Alias signal suppression	>30 dB	Yes
Dynamic range	39 dB	Yes, 39 dB 100 MHz both bands 320 MHz C-band 37 dB, L-band 38 dB

Outlook for further improvements

- Outlook for further improvements
- - automatic on chip adjustments
- - improvement of LO isolation
- - improvement of Noise Figure
- - improvement of ADC S&H

Improvement of LO isolation possible solutions

- All LO inputs differential
  - Now C & X differential; L single-ended
- C and X-band LO and RF feeds orthogonal
  - At the corners
  - L-band as now, in the middle (but perhaps differential input gives enough improvement)
  - Probably increases chip area; already quite pad-limited
- LO on-chip buffering after the polyphase filter
- Fractional LO feed (e.g. by /2 or /3)
  - And on-chip frequency multiplier

Conclusion

- A multi-band (L,C,X) receiver designed and realized
- C and L-bands operational, X-band heavy gain loss
- L and C-band values in specifications up to room temperature
  - over that input amplifier gain starts to drop under specs
    - cannot be fully compensated with gain control
- Greatest problem LO-RF leakage
  - large dc-offset
    - goes partially out of ADC input range
    - restricts control adjustments' usable range
- Improvements possible and presented

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