Fourth International Workshop on Analogue and Mixed Signal Integrated Circuits for Space Applications

IHP BiCMOS technologies for RF and mixed signal applications

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R.F. Scholz, F. Teply, M. Cirillo

IHP
Im Technologiepark 25
15236 Frankfurt (Oder)
Germany

Outline

Introduction

0.25µm BiCMOS – SGB25V/SGB25RH

- Technology description
- Evaluation Status
- Running radhard library project
- Other projects using SGB25V technology

0.13µm BiCMOS - SG13S

IHP in a Nutshell

- **Institute of the Leibniz Association**
  Owned by the State of Brandenburg; limited liability company since 1991

- **Founded in 1983**
  Long term experience in silicon technology & materials research

- **Silicon based high-frequency technologies, circuits and systems**
  for the wireless and broadband communication

- **300 people from 20 countries**
  Among them 139 scientists

- **Certified DIN EN ISO 9001:2008**

The IHP`s Building in Frankfurt (Oder)

Pilot Line

CLEANROOM SIZE	~ 1000 m² Class 1
TECHNOLOGY	RF SiGe:C BiCMOS
WAFER SIZE	200 mm
CAPACITY	100 Wafer Starts / Week
TOOL SET CAPABILITY	0.25µm / 0.13 µm
MODE OF OPERATION	24h, 7 Days / Week
SiGe:C BiCMOS Cycle Time	≥1.7 Days / Mask level

Application Specific Integrated Circuit (ASIC) development flow

ASIC Design

IP- IHP System/Circuit Design / Design partner Arquimea Ingenieria, Madrid

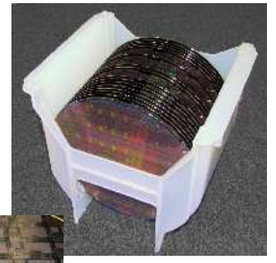
Prototyping (MPW) Test, Redesign

MPW run
Several customer share one wafer

Customer 1 Customer 2 Customer 3

Fabrication

Engineering run

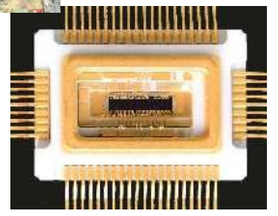


On wafer test

Performed in IHP Labs

Assembly & final test

Organized with external partners Cicor/RHe Micross UK



Technology Roadmap (complete technologies)

Development (no access for external customer)

Early access (MPW access, electrical parameters stable, not complete fixed)

Qualified

Space evaluated

Phase out (2 years MPW access for running projects)

Process	Features f_T/f_{MAX}[GHz]/BV_{CE0} [V]	2012 Q1 Q2 Q3 Q4	2013 Q1 Q2 Q3 Q4	2014 H1 H2	2015	
SGB25V	75/95/2.4, 45/90/4, 25/70/7					0.25 µm
SGB25RH (SGB25V)	75/95/2.4, 45/90/4, 25/70/7					
SG25H3	120/140/2.4,110/180/2.3, 45/140/5, 30/80/7					
SG25H1	190/190/1.9, 180/220/1.9					
SG13S	250/300/1.7, 45/120/3.7					0.13µm
SG13RH (SG13S)	240/300/1.7, 50/120/3.7					
SG13G2	300GHz/ 500GHz /1.6 (no digital libs)					

August 2012

MPW Schedule 2012

TAPE IN	Shipment	SGB25		SG25		SG13	
		V	RH	H1	H3	S (C)	G2
Dec 12, 11	20 Apr, 12					x	x
Jan 09, 12	Apr 02, 12	x		x[1]	x		
Apr 16, 12	Aug 27, 12					x	
Apr 30, 12	Jul 23, 12	x		x[3]	x		
Jul 30, 12	Nov 19, 12					x	x
Sep 03, 12	Nov 27,12	x	x[2]	x[1]	x		
Nov 05, 12	Feb 11, 13	x	x[2]	x[1]			
Dec 10, 12	19 Apr, 13					x	x

1 Shipment 7 days later
2 Shipment 21 days later
3 Run without priority

TAPE IN	Shipment (standard)	GD	H3P	RF-MEMS switch[1]	LBE[1]	Cu Plating (with IZM)[2]
Jan 09, 12	May 14, 12		x	x	x	
Apr 30, 12	Aug 27, 12	x		x	x	x
Sep 03, 12	Jan 07, 13		x	x	x	x
Nov 05, 12	March 11,13	x		x	x	x

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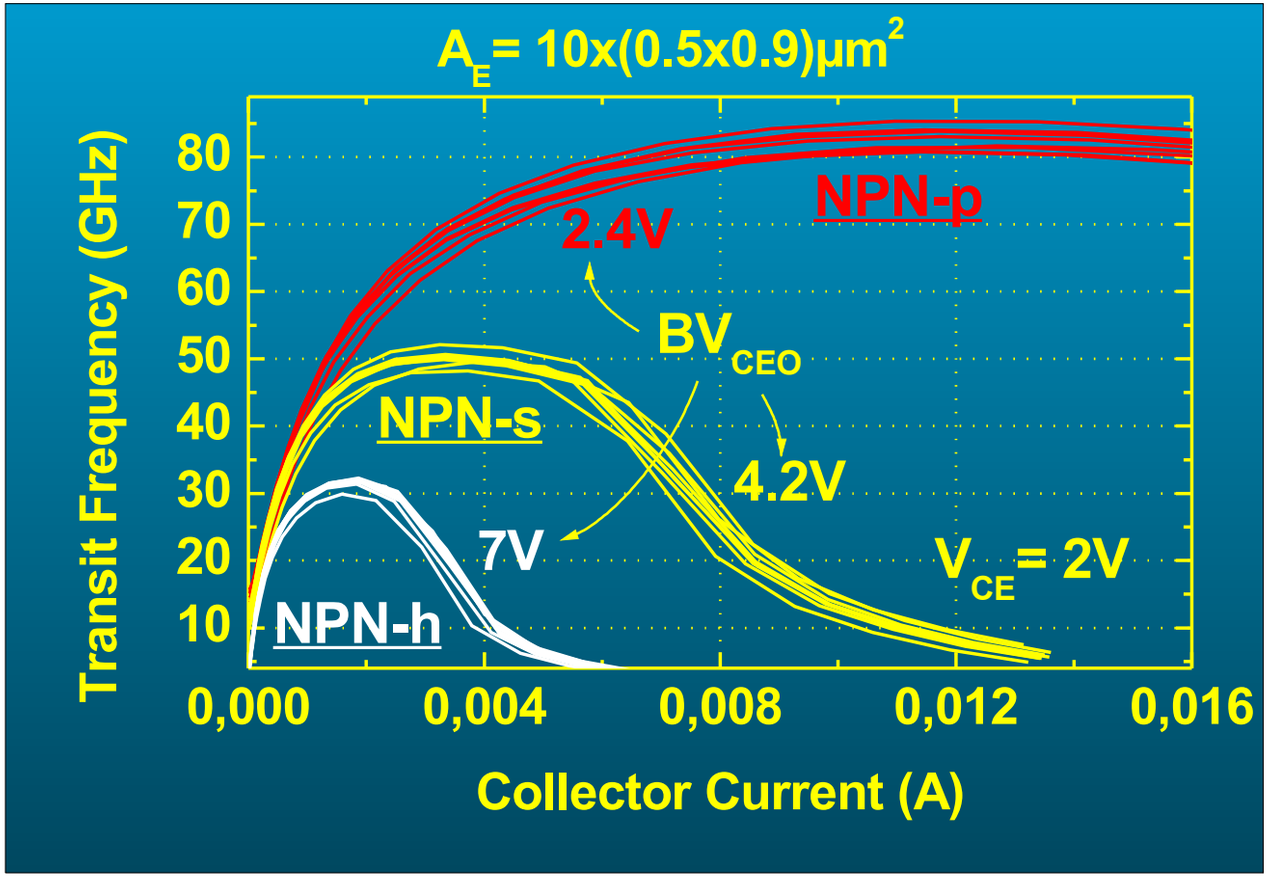
SGB25RH Process Options

Features	SGB25V / SGB25RH Full BiCMOS
Bipolar (fT/fmax/BVCE0)	High-speed HBT: 80 GHz/ 100 GHz/ 2.4 V Medium-voltage HBT: 45 Ghz/ 120 GHz /4 V High-voltage HBT: 28 GHz/ 120 GHz/ 7 V
CMOS	Vdd=2.5V, Tox=5nm
CMOS logic	Digital libraries
Passives	Poly-Si resistors, MIM capacitors, MOS varactors, a.o.
Interconnects	5 layer Al incl. 2µm & 3µm thick layers

SGB25V/SGB25RH (1-mask) HBT Construction

There are 3 HBTs differing in BV_{CEO} and peak f_T

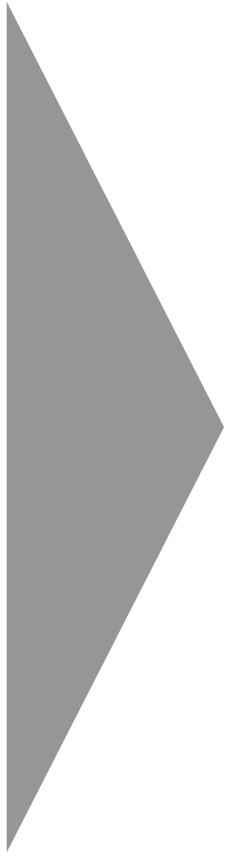


The different curves explain the typical scattering across an 8'' wafer

SGB25RH Elements and Applications

Basic structure elements:

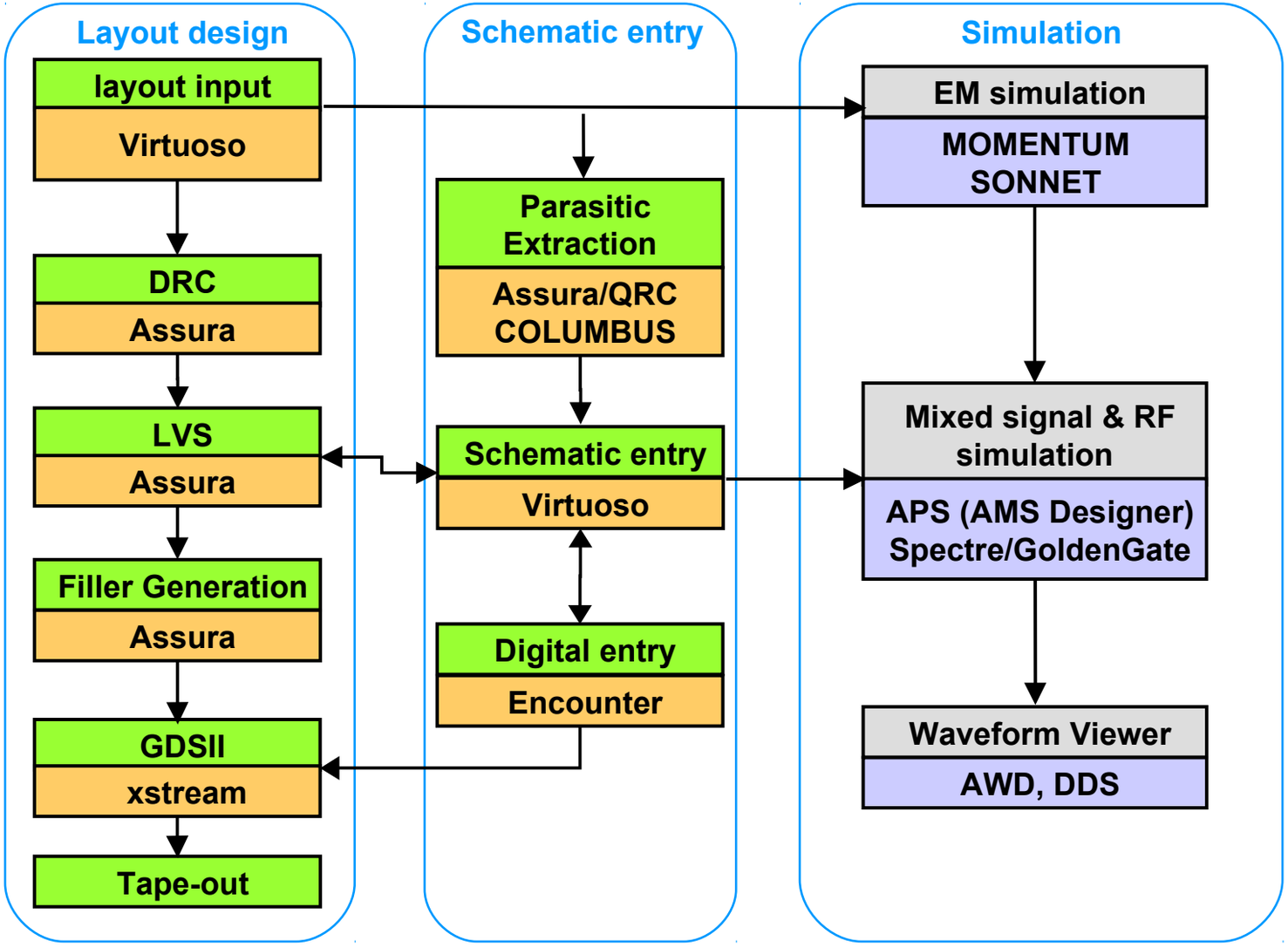
- PMOS
- NMOS
- I solated NMOS
- MOS Varactor
- RPND resistor
- RSIL resistor
- RPPD resistor
- RHIGH resistor
- MIM Capacitor
- npnVS bipolar HBT
- npnVH bipolar HBT
- npnVP bipolar HBT
- Inductor made by backend metal layer
- Antenna diode
- ESD clamp
- Digital standard cells
- Digital IO cells



Components in CMOS, bipolar and BiCMOS

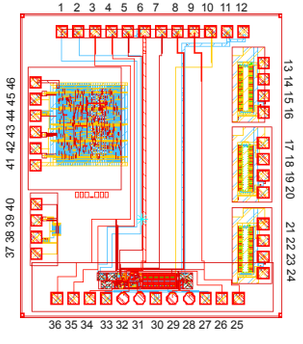
- Maximal application frequency up to 20 GHz
- as chip or packaged
- Mixed Signal Technology
- fast counters
- fast shift register
- FlipFlops
- Dividers
- Frequency-/Phase comparator
- Charge pumps
- VCOs
- Linear amplifiers
- Current sources
- PLLs (integer and fractional)
- Digital Analog Converters
- etc.

IHP Cadence DFII Design Flow

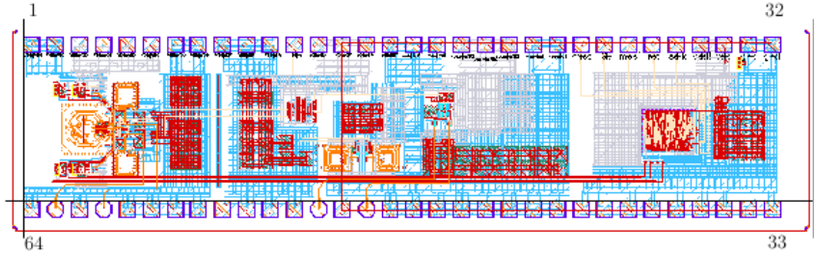


Test vehicle evaluation by DLR/ESA

TCV – standard technology test segments packaged in DIL64 (HBTs, NMOS, PMOS, resistors, MIM, MOS varactor, diodes



DEC – Circuit blocks in Strategie 64 pin RF package (CMOS RO, CMOS shift register, bipolar ROs, ECL shift register with internal VCO)



RIC – 20 GHz VCO with divider, 6GHz output and SPI interface to control frequency, KYOCERA package

Status of SGB25RH evaluation

- TCV: 4000 hours passed, Expected failures occurred, test report available, 250°C storage test OK but gold wire packages fail, 275°C storage test up to 500h OK, 125°C storage test in package OK
- RIC:Long term stress test passed 4000 hours without errors
- DEC: 2 step stress done without errors as of May 2012, 2 more to do, Long Term stress to be done afterwards
- All tests (DEC) finished end of 2012
- Parts for DPA sent to ESA
- DLR/ESA Audit performed successfully 19th/20th of October 2011
- Final Goal IHP technology in preferred part list

Radiation test Data SGB25V/SGB25RH

• Teply et. al.: Radiation Hardness Evaluation of a 0.25 µm SiGe BiCMOS Technology with LDMOS Module, RADECS 2011 Data Workshop, available online at IEEE Xplore

• Kayser-Threde: Radiation Test Report - TID on early Structures (30-20-RP-KT-001_2)
• Kayser-Threde: Radiation Test Report - SEE on early Structures (30-20-RP-KT-002_2)
• Kayser-Threde: Radiation Test Report - TID Verification LO7 (3020-RP-KT-005)
• Kayser-Threde: Radiation Test Report - SEE Verification LO7 (3020-RP-KT-006)

Additional activity:
Test of Radhard library in SGB25RH

- New DRC Rules on Transistor Level
  - Disabling of Latchup Rules is Forbidden
  - Gate Poly extension of MOS gate is limited
  - PWell and Nwell contact rings must have limited dimensions
  - All Devices must be located within contacted NWell/PWell Ring
  - Gate Poly have not to cross any well border
  - Gate Poly must be within NWell or Pwell
  - Active Shapes on different nets must be shielded with well contact

- Applied in Dolphin cell library and integrated the standard Cadence design flow

Evaluation of Radhard Library

Goal :

- Design Test structures to characterize each types of Single Event Upsets

Categories of Test Structres :

- Register cells : FlipFlops, latches, RAM
- Combinational Logics: Using NAND/NORS
- Special Structres: IO, Bandgap circuits
- Test pattern – Generator/ion
- FPGA / Labview

Radiation Tests :

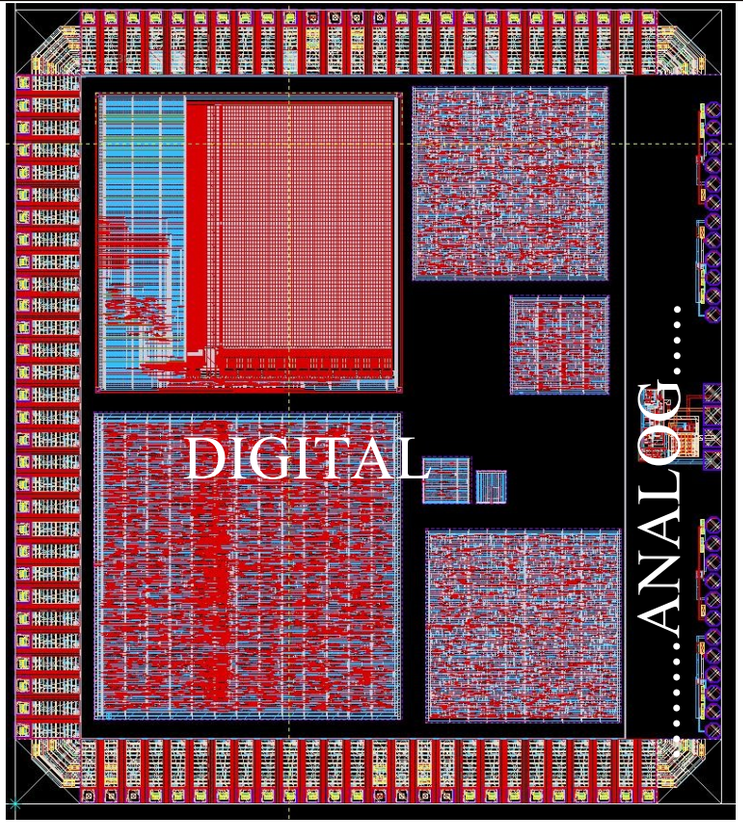
- Heavy ion tests with effective LETs ranging from 1.8 MeV*cm²/mg to >80 MeV*cm²/mg

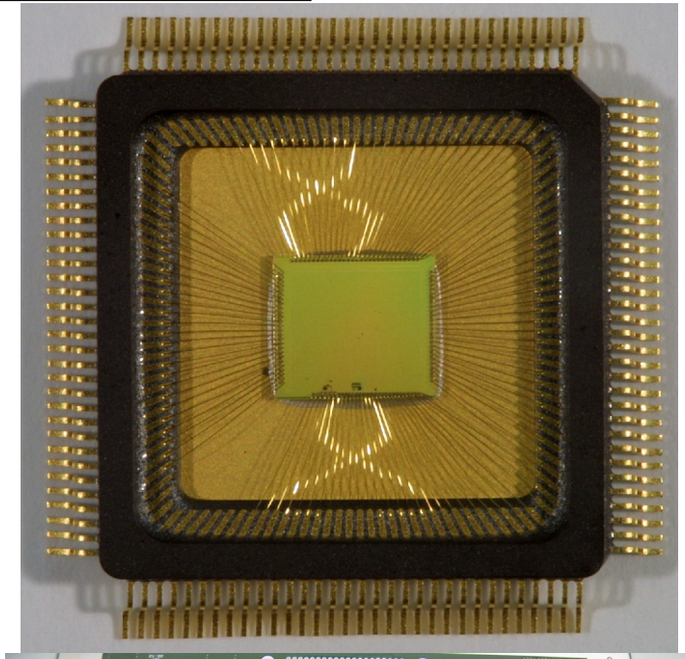
Test Structures

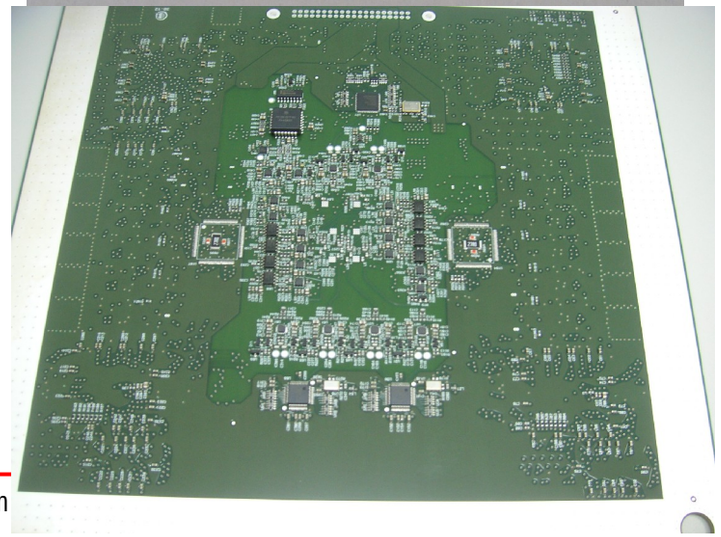
	TEST STRUCTURES	MEASUREMENT
1	Registers	
a	Static shift registers - Stages 2048	
b	Dynamic Shift Registers - 1024	
2	Ring Oscillators	
	1000+1 stages	Operational frequency and power consumption Inverter propogation delay, Tpd with Varying LETs, Power delay wrt VDD with Varying LETs
3	SRAM	Transient Faults Static and Dynamic Modes of operation Single Bit and Multi Bits Upset Distribution SEUs (varying VDD and Temperatures over LET)
4.	IO - LVDS	
5	ECL Shift Registers	
6	Bandgap Reference	

All digital stuctures are variants : sgb25_cell , sgb25rhd_cell, TMR

Chip Layout/Package for SEU Tests







Radiation campaign including board design will be performed in September by ARQUIMEA Ingenieria, Madrid

Space projects in SGB25V/SGB25RH

ARQUIMEA (Spain – Prime Contractor) : "EUROPEAN LVDS DRIVER Incl. COLD SPARE CAPABILITY; DEVELOPMENT AND ESCC EVALUATION AND QUALIFICATION " - ESA Tender AO/1-6922/11/NL/LvH."

Project Consortium :

Design and Programme Management : ARQUIMEA (Spain)

Technology Provider : IHP (Germany)

Assembly House : Micross (UK)

Test House : Alter Technology Group (Spain)

Full Duration : 30 Months (for Phase I to Phase III)

Objective : Rad-Hard LVDS ICs with the following functions :

- **Dual LVDS Transceiver pair IC** compatible to NS DS90LV049Q Automotive part.
- **4x4 LVDS cross point IC** compatible to TI NS65LVDS125 commercial part.

Space projects in SGB25V/SGB25RH

Space Engineering (Italy) : “HIGHLY INTEGRATED BFN USING ON CHIP MULTINODE CONCEPT” - ESA Tender AO/1-5920/08/NL/ST.”

Current SiGe MMIC technology, allows the design of multinode MMICs integrating more than one beam-forming node on the same chip. The technology allows also the integration of mixed analogue/digital functions on the same chip, thus significantly reducing the complexity part count, yield and overall cost of BFNs for both multibeam reconfigurable payload/antennas and for phased array mobile terminals

Democritus University of Thrace (GREECE): Essential TeleMetry (ETM) support ASIC

Thales Alenia Space (France) partly CNES funded, IHP as subcontractor

Kayser Threde/IHP (Germany): Fractional-N Synthesizer, 12 bit DAC 1.5Gsamples

IHP (Germany): DLR funded, Middleware Switch

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CMOS	Vdd=1.2 V, Tox=2 nm + Vdd=3.3 V, Tox=7 nm
CMOS logic	Digital libraries
Passives	Poly-Si resistors, MIM capacitors, MOS varactors, a.o.
Interconnects	7 layer Al incl. 2µm & 3µm thick layers

Companies and institutions supporting this initiative

- Kayser Threde
- Jena-Optronik
- Advico GmbH
- IMST GmbH
- Astrium
- Dolphin Integration
- Tesat

DLR project:
Evaluation of a radhard library and ESCC test structures in 0.13µm BiCMOS

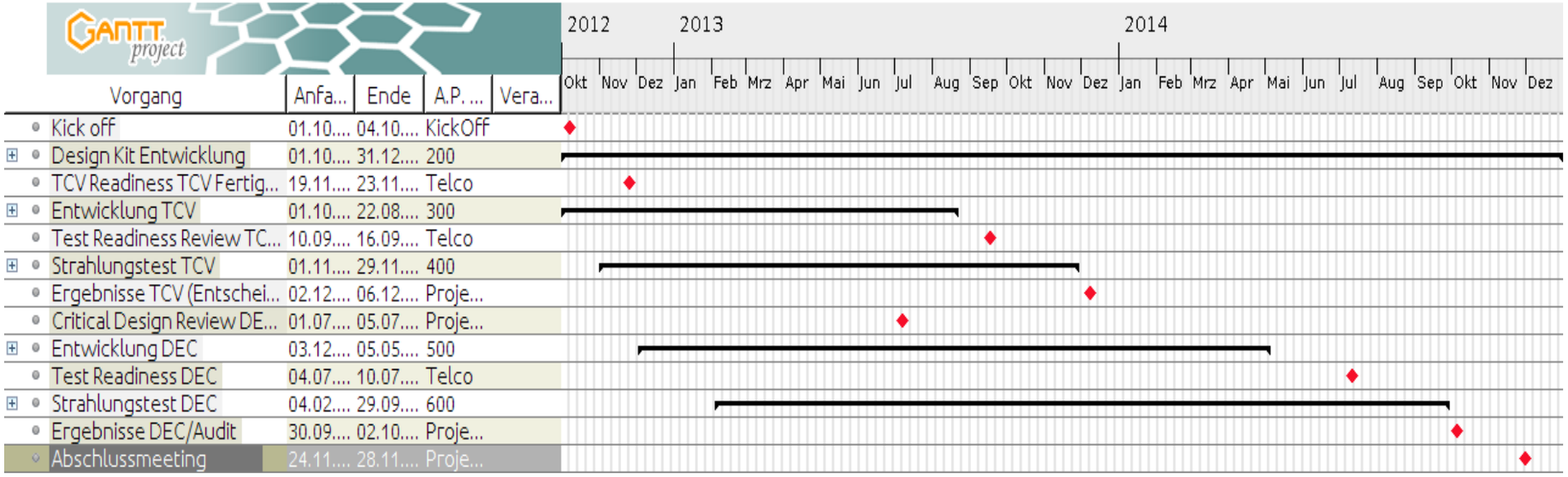
Goals:

- SG13 Technology radiation evaluation for Space applications
- Target RF mixed signal application up to 120 GHz
- Low power digital designs

Workpackages:

- Mixed Signal BiCMOS DesignKit with radhard digital IP
- Development and radiation test of TCV teststructure
- Development and radiation test of DEC teststructure

General overview project proposal
0.13µm mixed signal technology



Vorgang	Anfa...	Ende	A.P. ...	Vera...
Kick off	01.10....	04.10....	KickOff	
Design Kit Entwicklung	01.10....	31.12....	200	
TCV Readiness TCV Fertig...	19.11....	23.11....	Telco	
Entwicklung TCV	01.10....	22.08....	300	
Test Readiness Review TC...	10.09....	16.09....	Telco	
Strahlungstest TCV	01.11....	29.11....	400	
Ergebnisse TCV (Entschei...	02.12....	06.12....	Proje...	
Critical Design Review DE...	01.07....	05.07....	Proje...	
Entwicklung DEC	03.12....	05.05....	500	
Test Readiness DEC	04.07....	10.07....	Telco	
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Ergebnisse DEC/Audit	30.09....	02.10....	Proje...	
Abschlussmeeting	24.11....	28.11....	Proje...	

- Radhard library is available
- Start October 2012 till December 2014
- Additional ESA funding possible in 2013 for complete evaluation in case of good test results from DLR project

Conclusion

- **IHP targets to offer its SiGe BiCMOS technologies as foundry service for Space applications**
- **Evaluation of 0.25µm BiCMOS technology nearly finalized**
- **Running Space Projects in 0.25µm BiCMOS**
- **Radhard and ESCC evaluation for 0.13µm BiCMOS will be started October 2012**