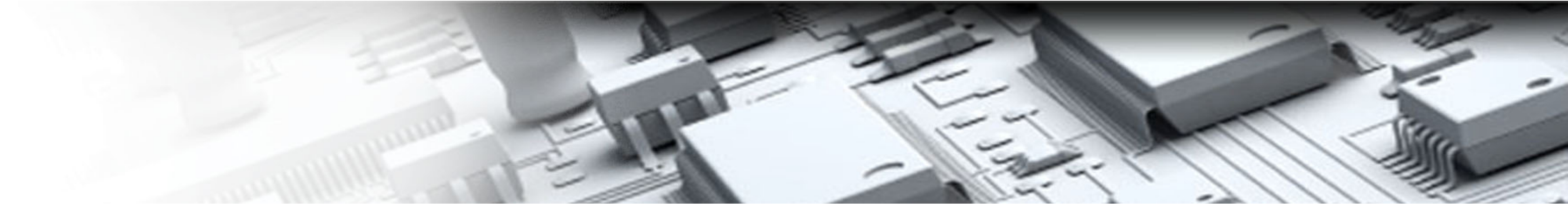

# Radiation Test of TFSMART2 Technology using Extended Common Mode LVDS and DC-DC Converter Components

**Volodymyr Burkhay(1), Gürkan Ilicali(2), André Rocke(3)**

**TELEFUNKEN Semiconductors GmbH & Co. KG, Germany**

(1)volodymyr.burkhay@telefunkensemi.com

(2)guerkan.ilicali@telefunkensemi.com

(3)andre.rocke@telefunkensemi.com

## AMICSA 2012

*International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications*

**August 28th, 12:00 – 12:30**

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# Outline

- Introduction
- TFSMART2 Technology Overview
- Tested Components
- Test Method
- Results and Discussions
- Conclusion
- Outlook

# Introduction

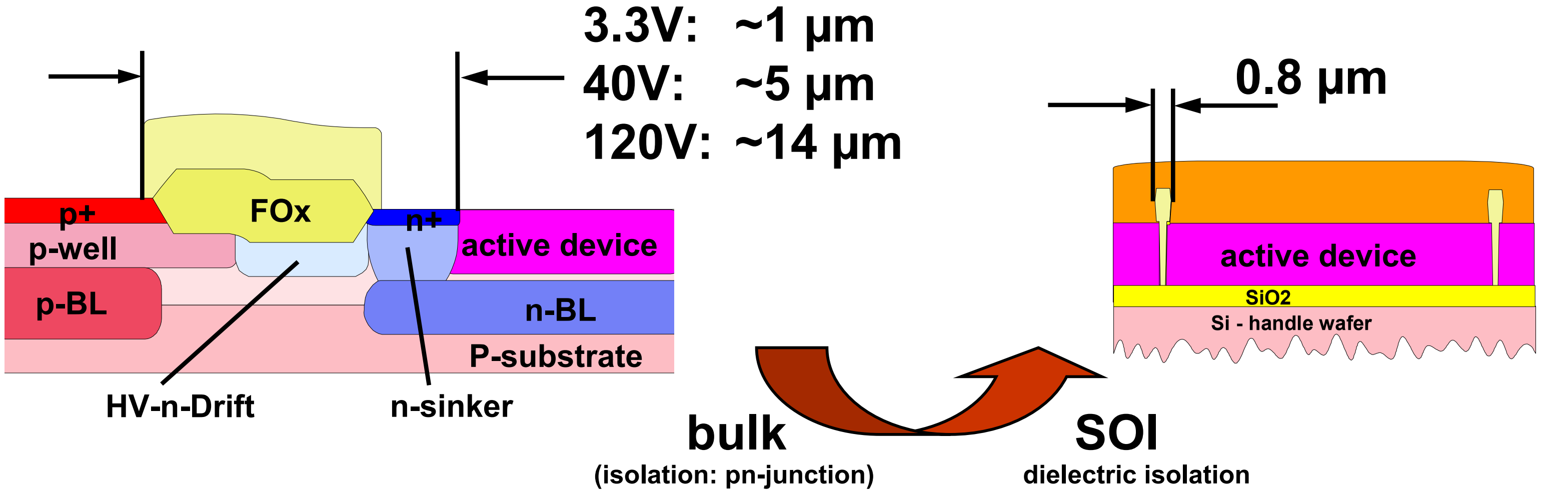
## Motivation

- Extend customer base towards high quality niche markets
- Recognition of European aerospace market demand to overcome ITAR restrictions
- Take advantage of specialty SOI technology - suitable for harsh and radiation environments
- A number of developed commercial components interesting for the aerospace market

## Experiment

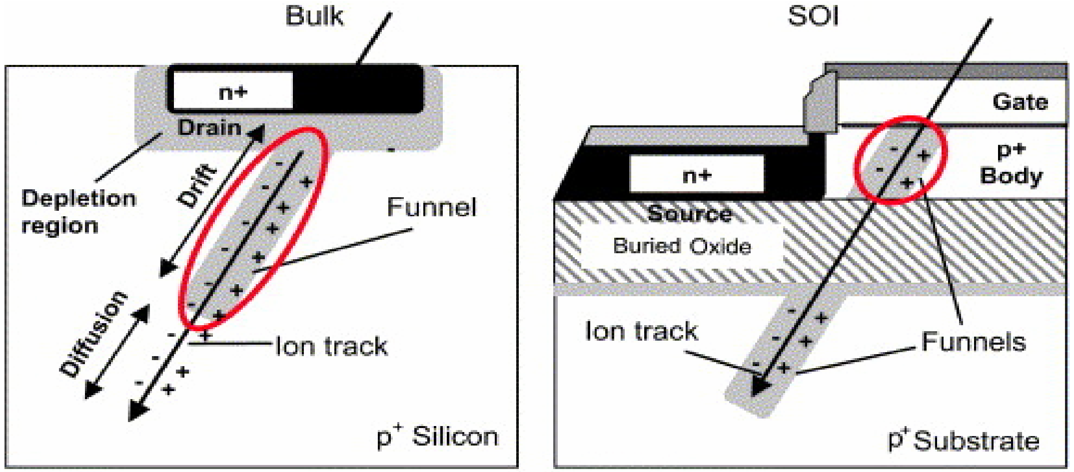
- Perform low-cost TID experiments up to 100krad
- Use existing commercial components

# Advantages of SOI



- Full dielectric isolation with deep trench
  - Enhanced integration density i.e. smaller chip size (more than 50% is possible)
  - Superior leakage control
  - Inherent prevention of latch-up
- Reduced substrate coupling
  - Enhanced device performance due to reduced parasitic coupling
  - High voltage capability, device stacking and even negative well voltages
  - Straight forward process flow and integration

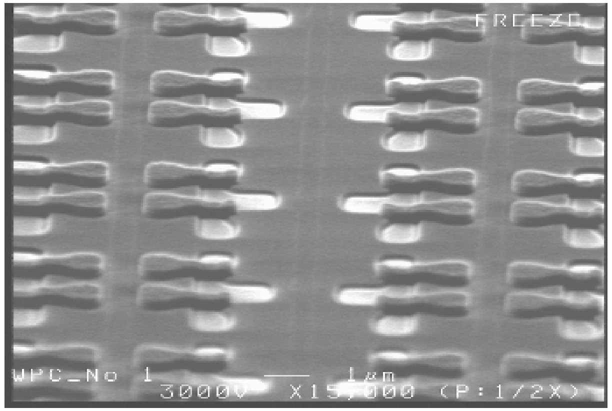
# Radiation Effects on SOI

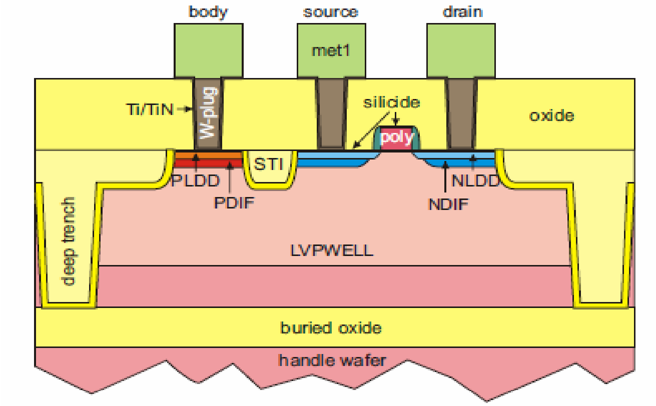


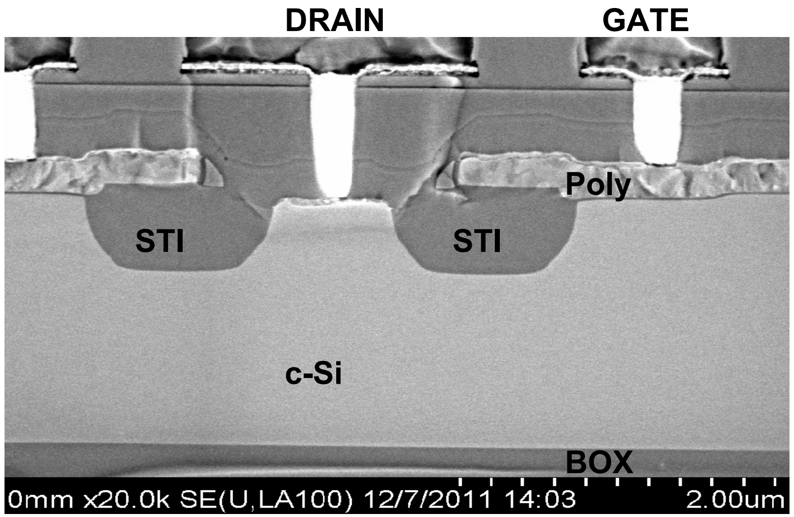
- SOI devices are known to be immune to SEL, which is a typical latch-up event triggered by prompt ionizing particles (ions, protons) entering into silicon.
- The body tie improves the single event immunity of SOI by providing the possibility to divert generated charges to the device ground.
- Other like SET and SEU can also be mitigated by the use of SOI due to much smaller charge collection volume compared to bulk devices.
- TID effects are mainly relevant to the insulator properties (gate oxide, buried oxide, trench isolations), which may impact various devices.

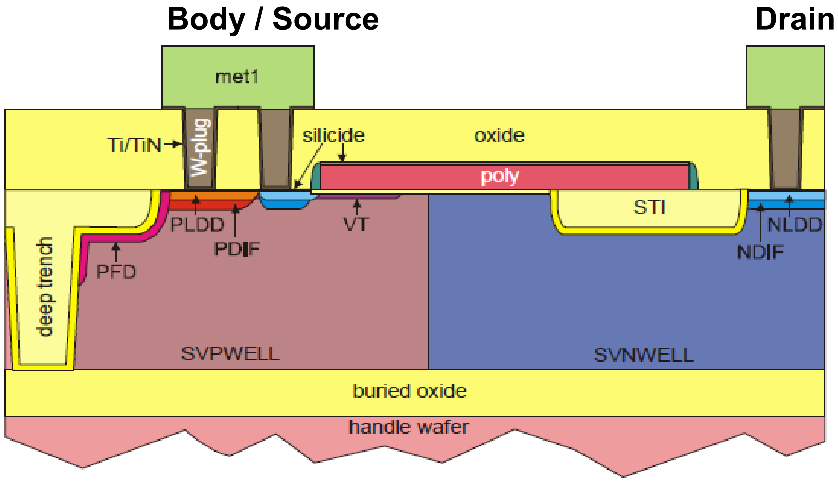
# TFSMART2

- The TFSMART2 is a 0.35µm BCDMOS technology platform combining bipolar, 3.3V CMOS logic and high voltage DMOS device components on SOI.









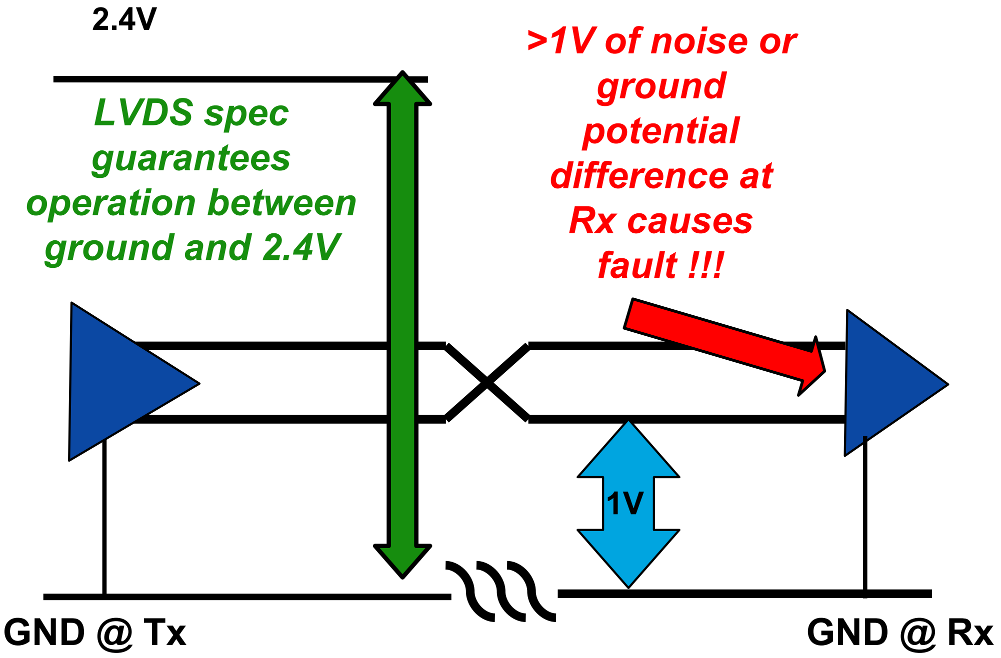
# Technology Features

| characteristic | details |
|---|---|
| minimum feature size | 0.35 µm |
| substrate | SOI ; p-type handle wafer <100> with 2 µm p-type <100> active layer |
| isolation | shallow trench, deep trench, buried oxide |
| well type | SV-NWell, SV-PWell; LV-NWell, LV-PWell |
| gate oxide | LV gate oxide 7.4 nm, HV gate oxide 17.5 nm |
| source/drain | LDD |
| metallization | 3 + 1 (metal 3 optional) level AlSiCu , tungsten contacts and vias, silicided contact areas, stacking of vias and contacts allowed |
| devices | Lateral NPN and PNP transistors<br>CMOS (3.3V, 5.0V)<br>HVNMOS (25V, 30V, 45V, 65V, 80V, 100V)<br>HVPMOS (30V, 45V, 65V, 80V)<br>6.2V Zener and 80V freewheeling and zapping diodes<br>11 different well, diffusion, low- and high-ohmic poly and metal resistors<br>5 different capacitors including GOX, poly and MIM |
| mask levels | 24 masks for base process with 3 metal layers |

# Tested Components

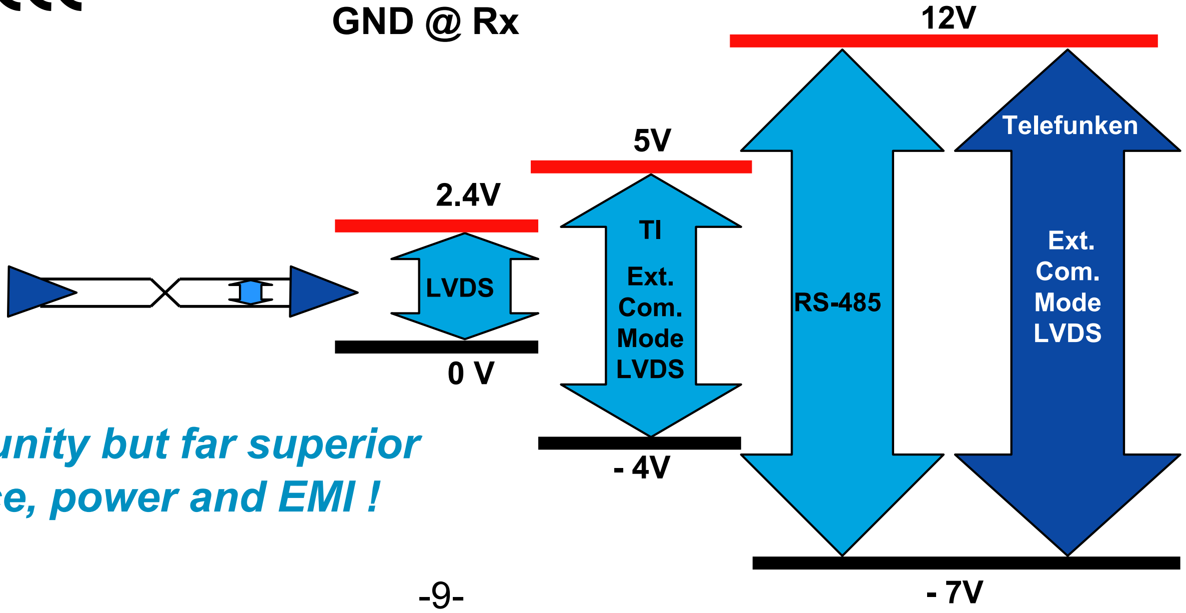
- Extended Common Mode LVDS
  - Driver TF90LVDS031
  - Receiver TF90LVDT032
  - Device utilization:
    - 3.3V high-speed and 5V MOS devices
    - Bipolar devices
    - ESD protection
- DC-DC converter
  - TF6002
    - 3.3V and 5V MOS devices
    - HVMOS devices
    - Bipolar devices
    - ESD protection

# Extended Common Mode LVDS



Box to box, command & control

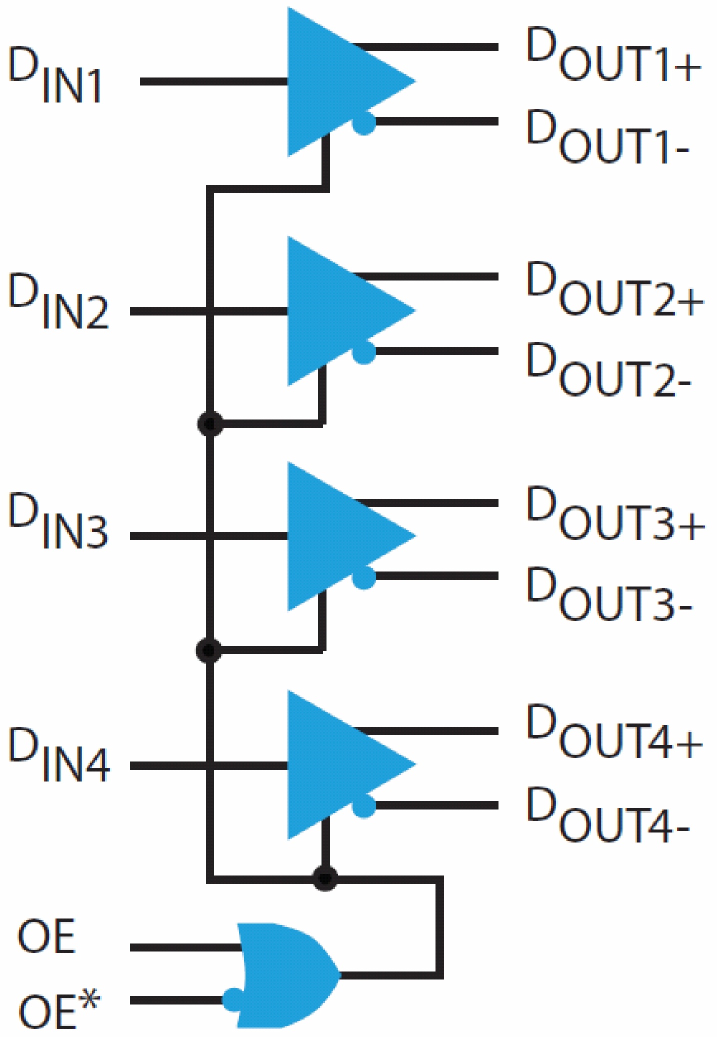
Ideal for box-to-box communication or noisy industrial, aerospace, signage & automotive applications



RS-485 noise immunity but far superior LVDS performance, power and EMI !

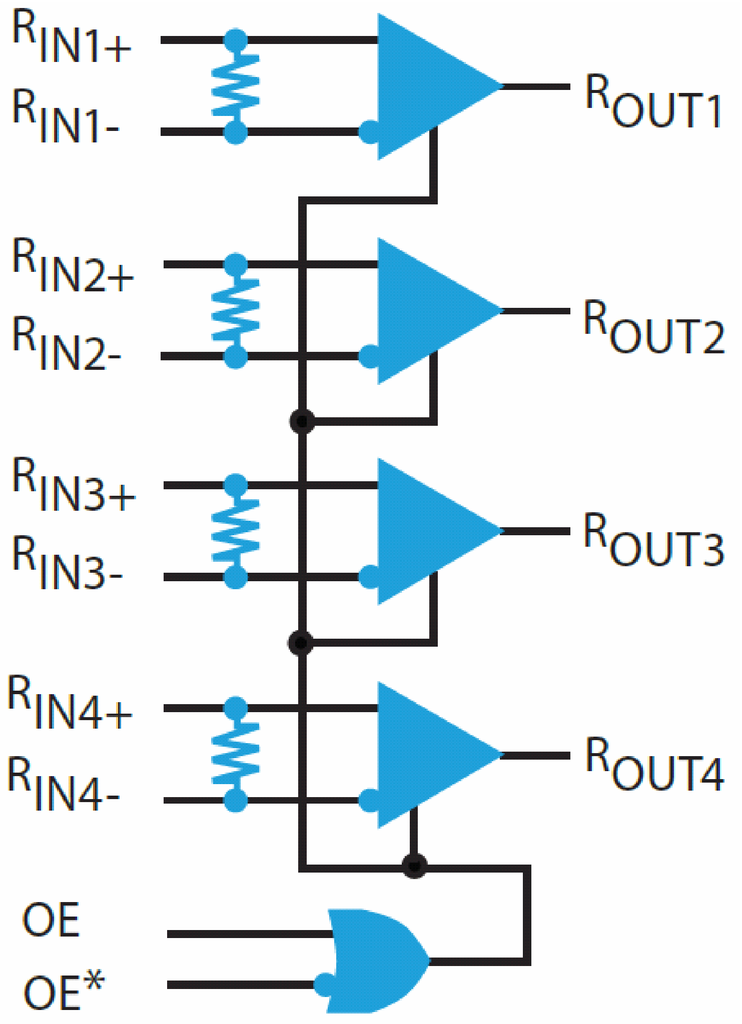
# TF90LVDS031

- 400Mbps Quad LVDS Line Driver
- 250ps max pulse skew
- 300ps max channel-to-channel skew (any edge)
- 23mA max supply current (loaded)
- -40°C to +85°C extended temperature range
- 16-pin SOICN package



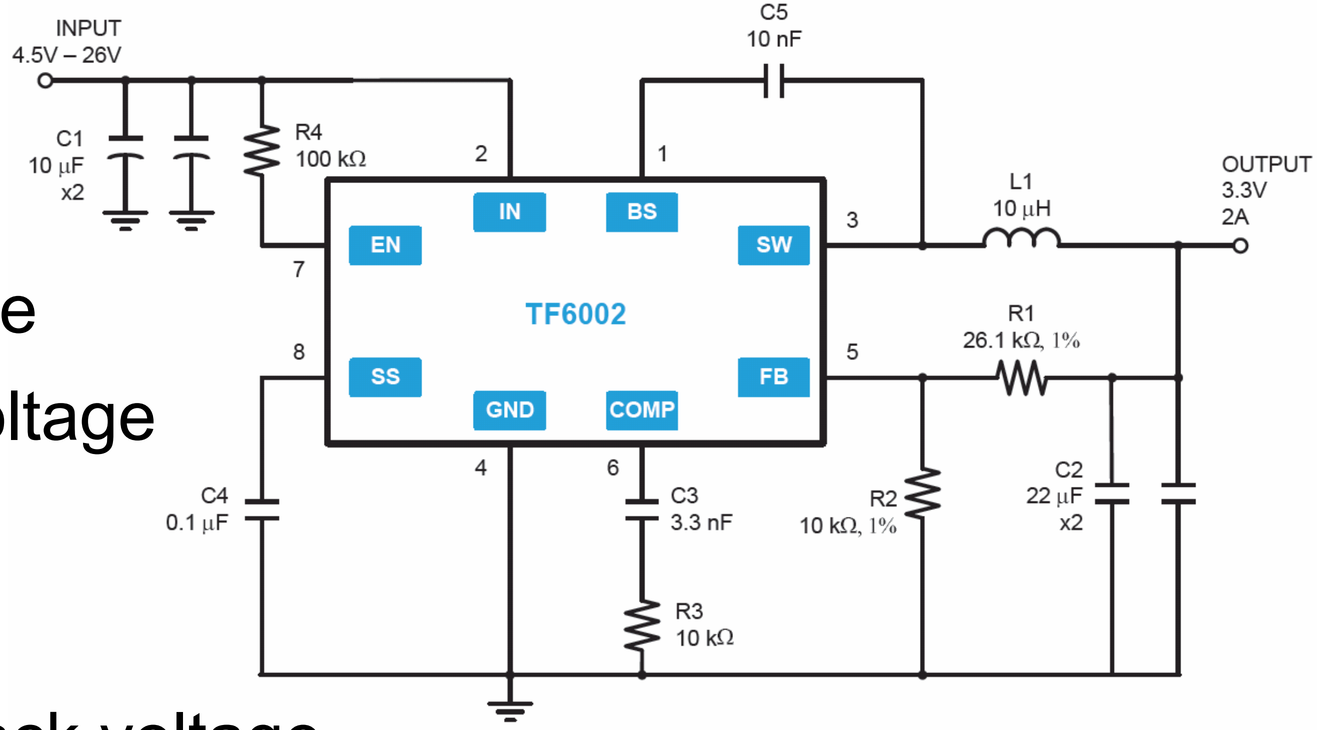
# TF90LVDT032

- 400Mbps Quad LVDS Line Receiver
- -7V to +12V extended common mode
- 100Ω on-chip termination resistors
- 300ps max pulse skew
- 400ps max channel-to-channel skew (any edge)
- 7mA max supply current
- -40°C to +85°C extended temperature range
- 16-pin SOICN package



# TF6002

- DC-DC converter
- 2A output load current
- 4.5V to 26V input voltage
- 0.923V to 23V output voltage
- 130mΩ MOSFETs
- >90% efficiency
- 2.5% variation of feedback voltage
- 340kHz fixed switching frequency
- 8-pin SOICN package
- -40°C to +85°C extended temperature range



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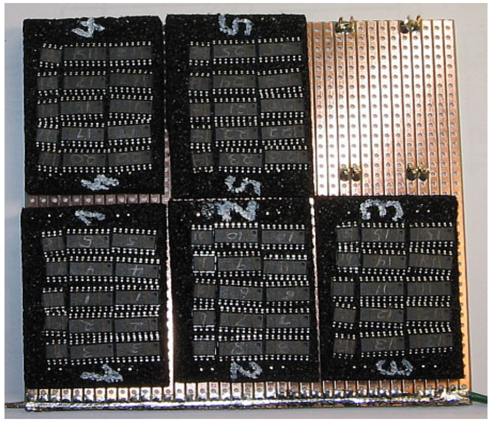
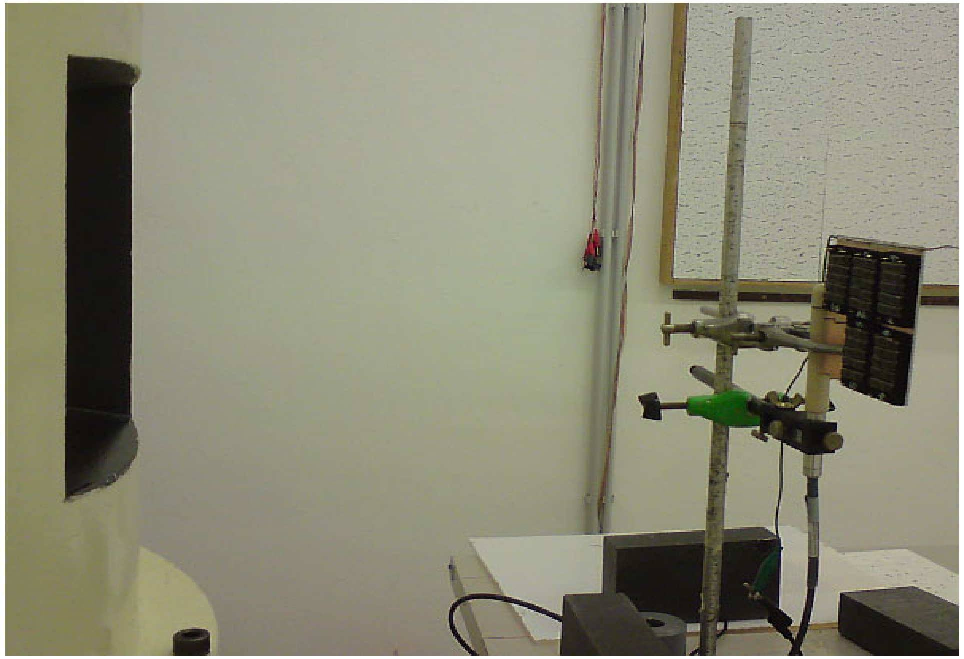
# Test Method

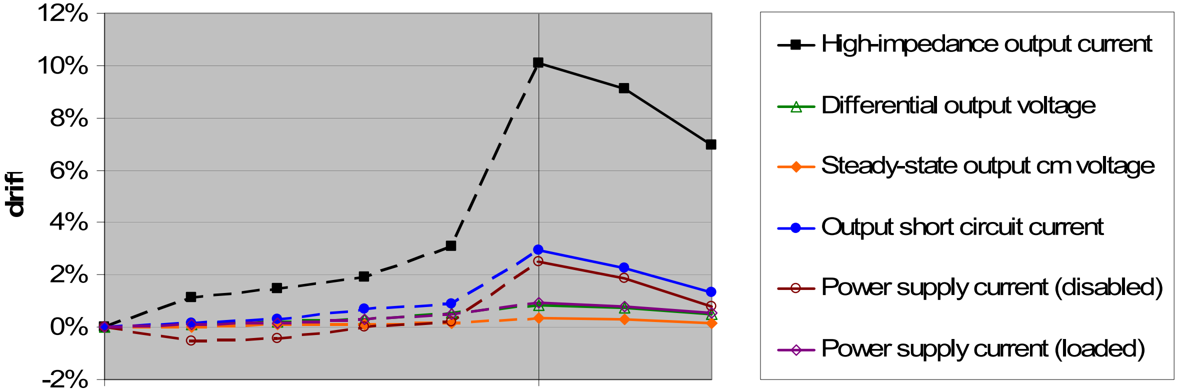
- Standard plastic packages
- Without applied bias
- 25 parts of each type
- 5 TID groups
  - 5krad
  - 10krad
  - 20krad
  - 40krad
  - 100krad
- Comparison groups
- Irradiation at ESTEC on 6-Mar-2012
- $^{60}$Co source
  - dose rate: 75 rad/min (distance 70cm)
- Room temperature annealing
- Hot temperature annealing 100°C for 5 h





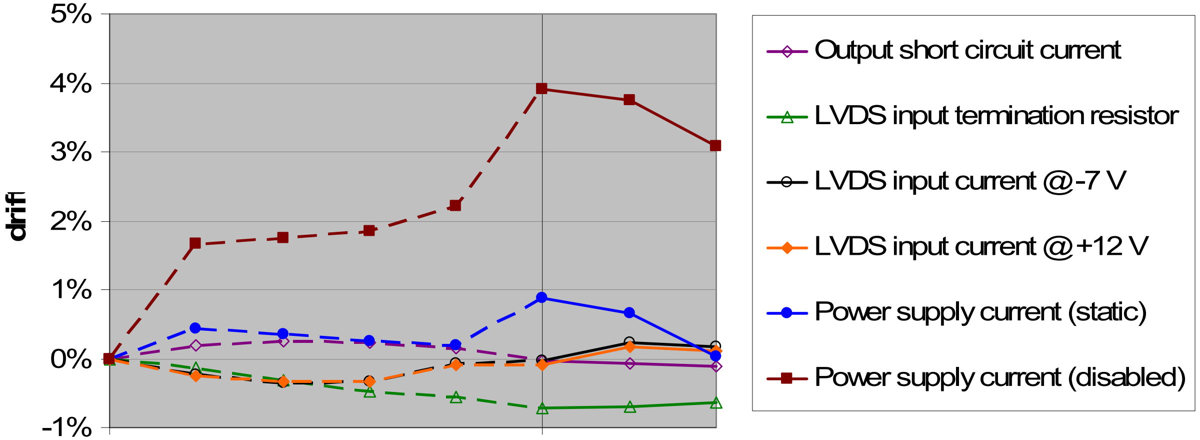
# Results Overview

TF90LVDS031



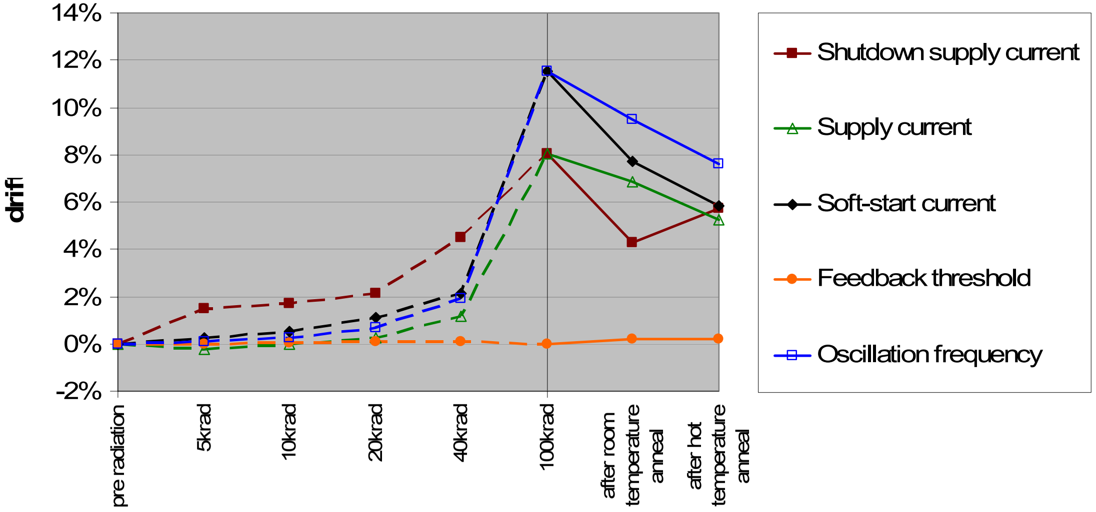
| Symbol | Dominant Dependency |
|---|---|
| *IOZ* | Process variation (MOS) |
| *VOD* | Mismatch |
| *VOCM* | Mismatch |
| *IOS* | Mismatch |
| *ICCZ* | Process variation and mismatch |
| *ICCL* | Process variation and mismatch |

TF90LVDT032



| Symbol | Dominant Dependency |
|---|---|
| *IOS* | Process variation (MOS) |
| *RIN* | Process variation ($R_{poly}$) |
| *IIN* | Process variation ($R_{poly}$) |
| *IIN* | Process variation ($R_{poly}$) |
| *ICCZ* | Process variation and mismatch |
| *ICC* | Process variation and mismatch |

TF6002



| Symbol | Dominant Dependency |
|---|---|
| *ISS* | Mismatch |
| *VFB* | Mismatch |
| *FOSC* | Process variation and mismatch |
| *ISD* | Process variation |
| *IIN* | Process variation and mismatch |

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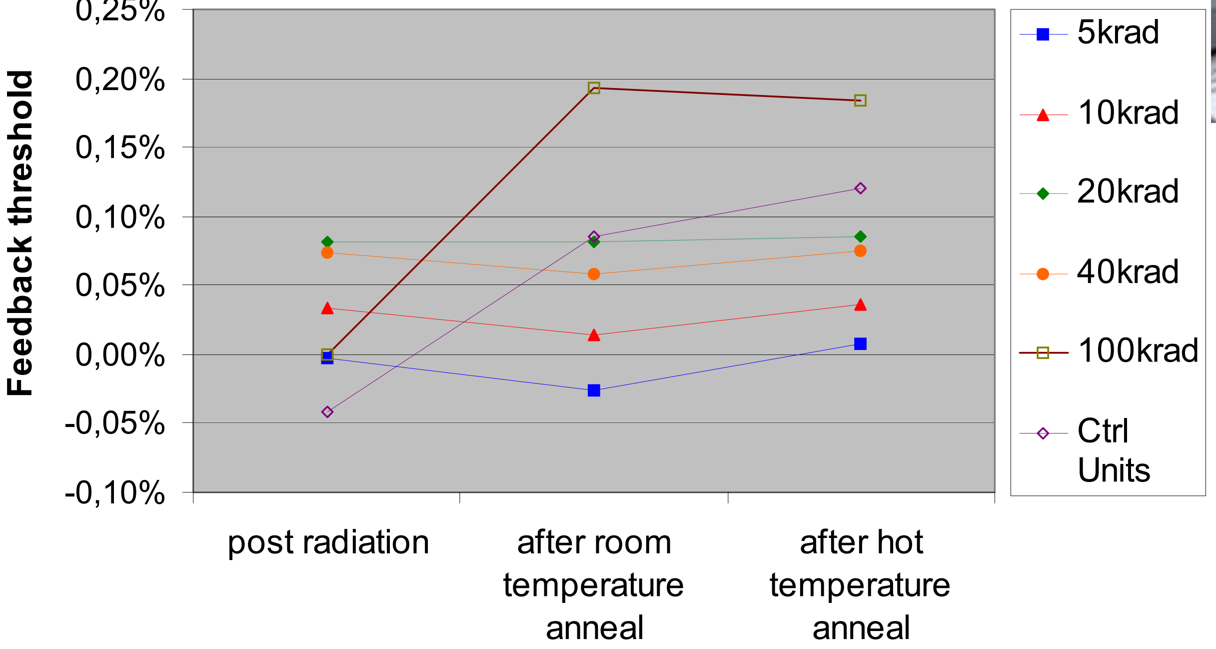
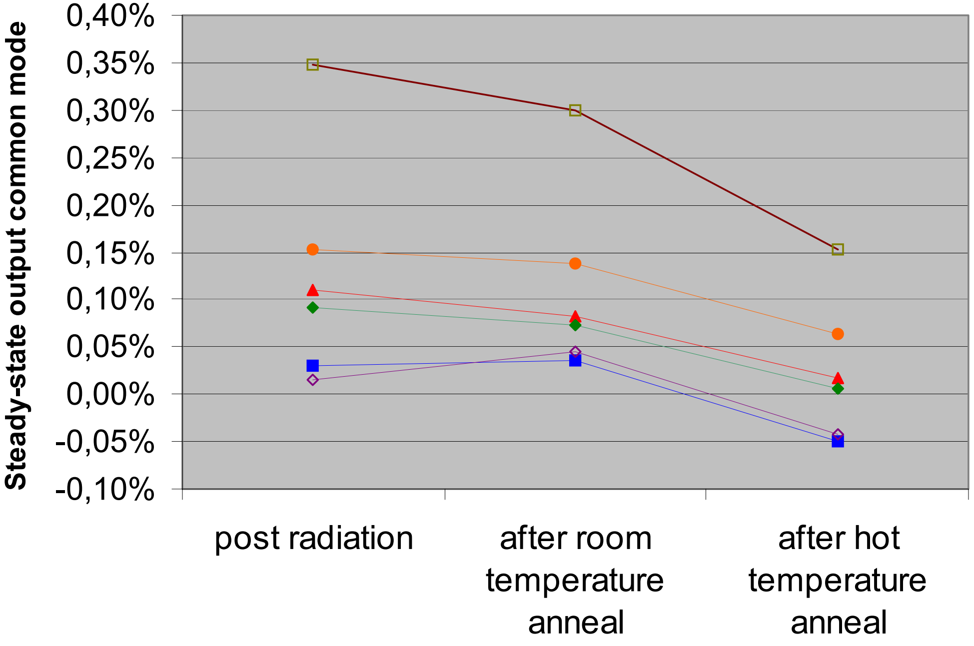
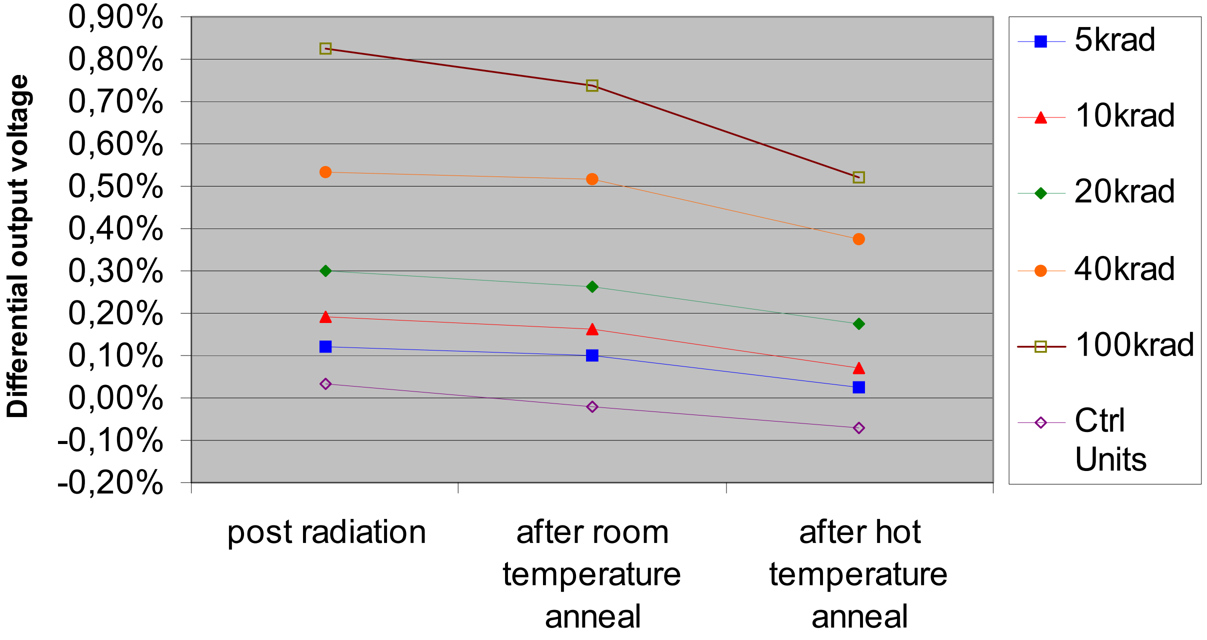
# Results

## Voltage Reference

- Bipolar mismatch
- Resistor mismatch
- Current mirrors


TF6002

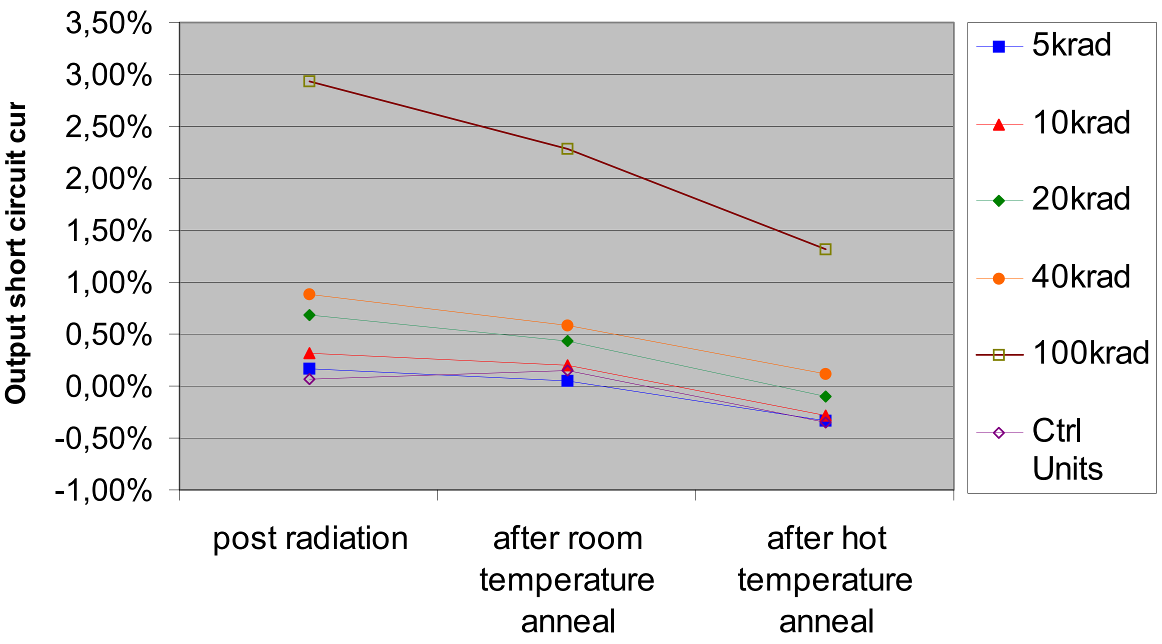

TF90LVDS031

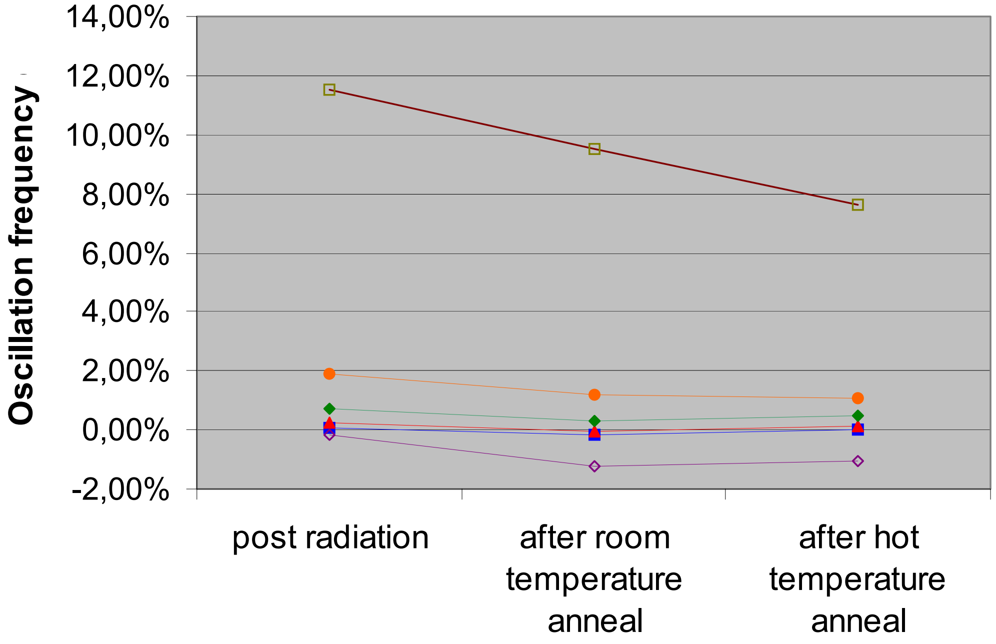

TF90LVDS031

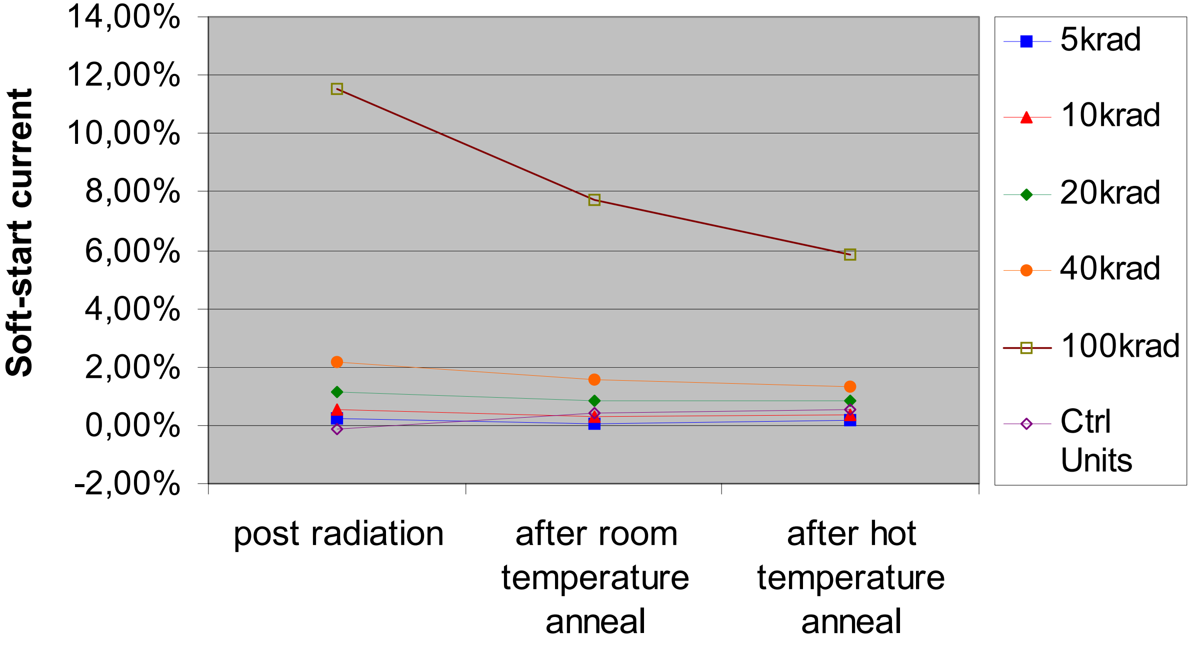
# Results

## Current Reference

- LV MOS mismatch
- 2 different circuit topologies


TF90LVDS031


TF6002

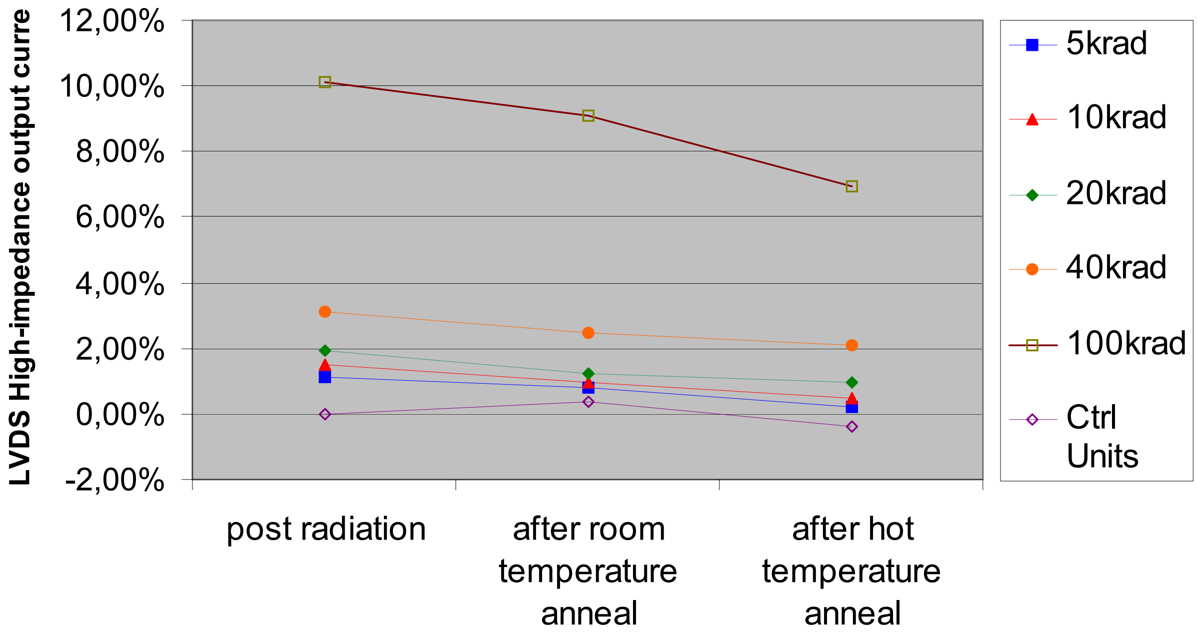

TF6002

# Results

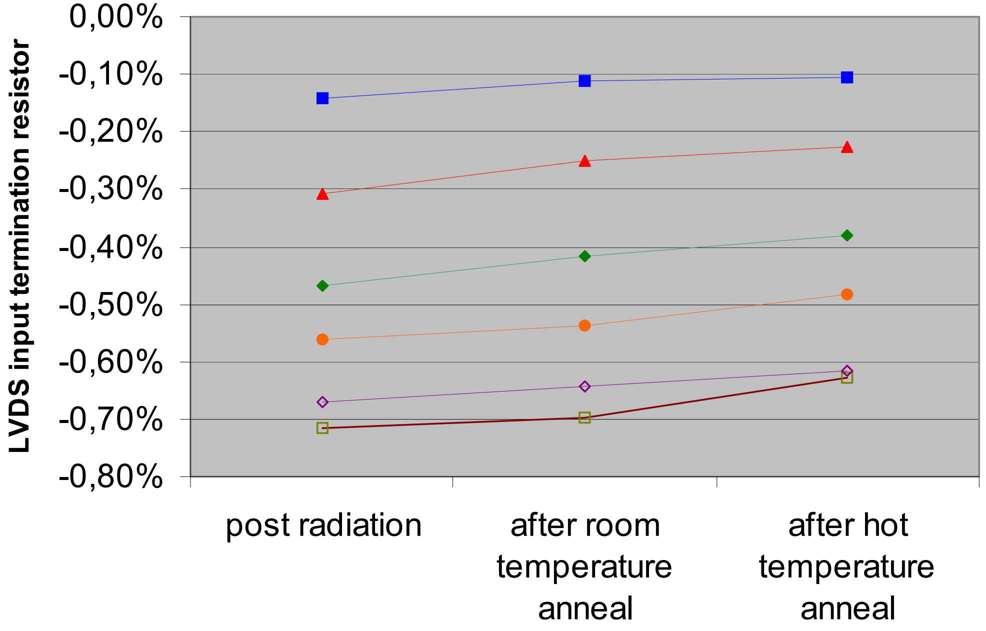
## Global Properties

- Rpoly is stable
- RDSon is stable
- Vth and probably other MOS parameters are drifting

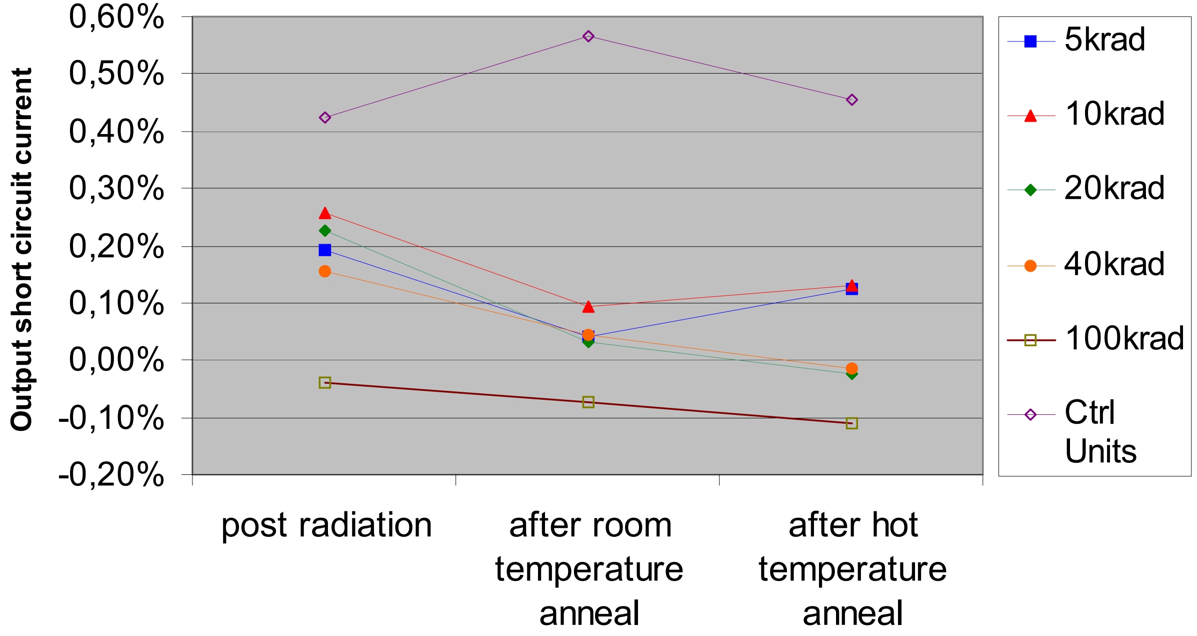
**TF90LVDS031**



**TF90LVDT032**



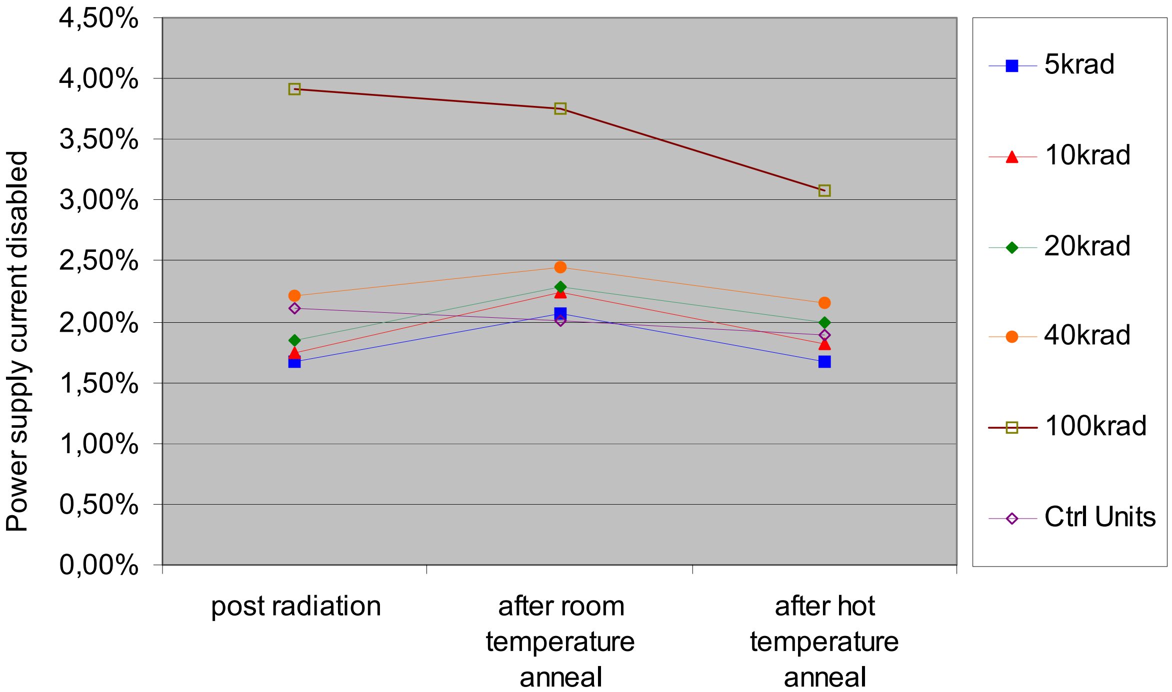
**TF90LVDT032**



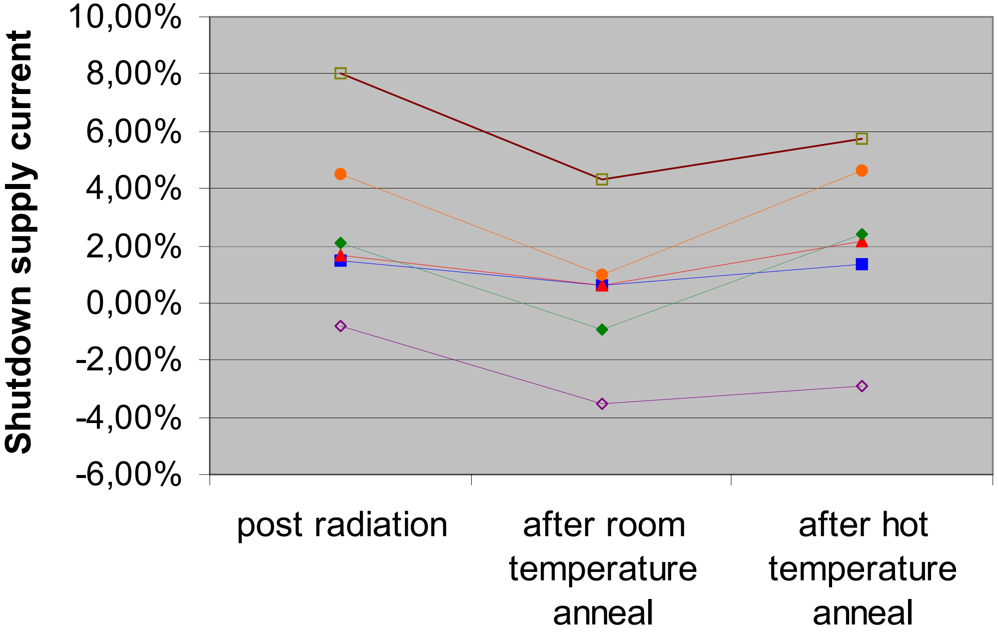
# Results

## Power Consumption

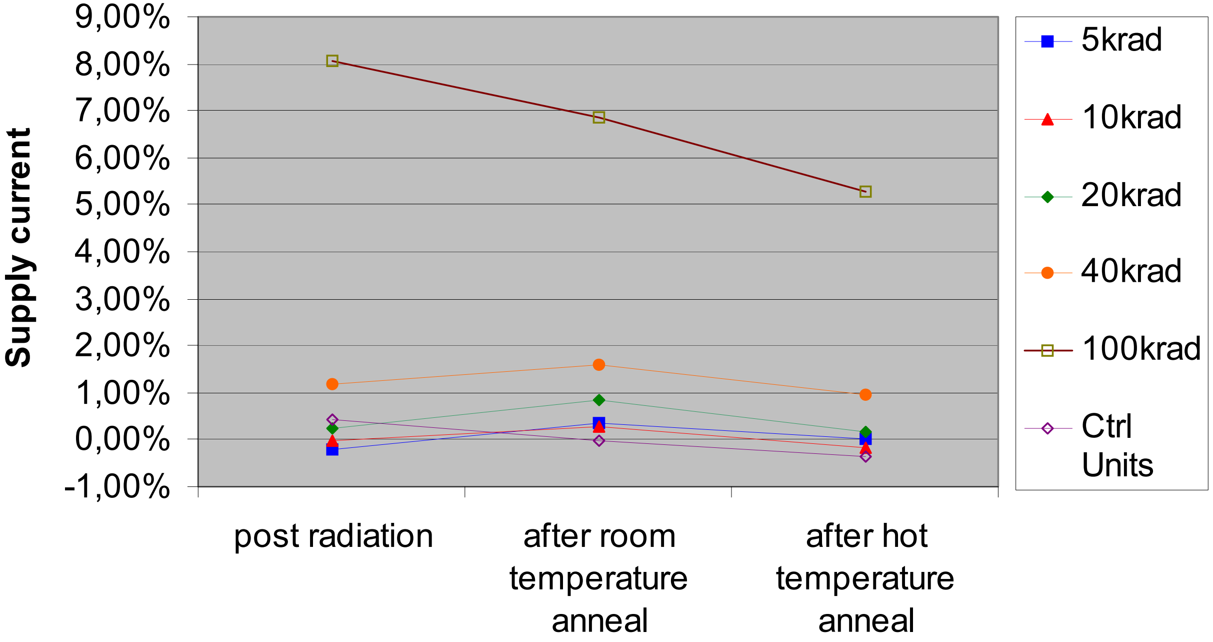
- Depends on different parameters
- Leakage increases


TF90LVDT032

TF6002



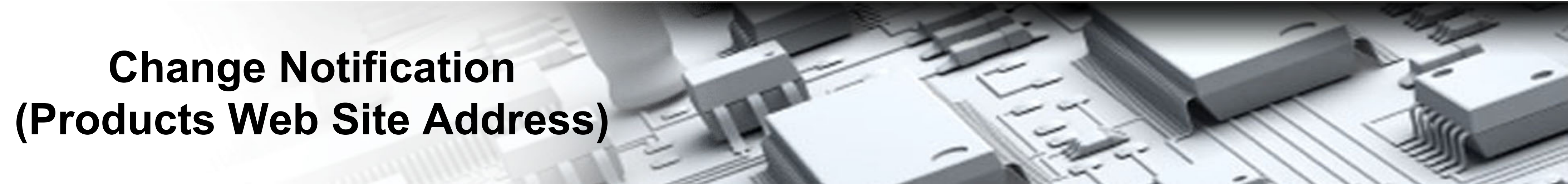
TF6002



# Conclusion

- Minor shifts in key data sheet parameters after TID irradiation up to 100krad
- None of the key component specifications are violated and remained well beyond the unacceptable limits; all tested parts keep their complete functionality
- TFSMART2 process and the tested circuit concepts have a great potential for the future aerospace applications

# Change Notification
# (Products Web Site Address)



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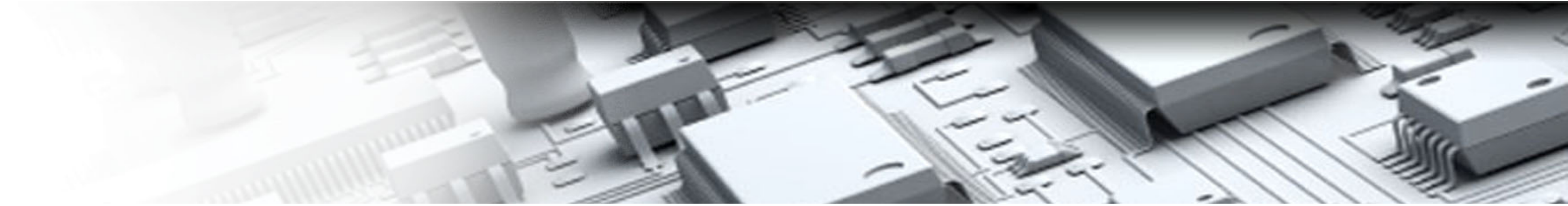

# *Thank you for your attention!*