

Barriers to Mixed-Signal Technology Growth in Space

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- Introduction
- Semiconductor Technology Development
- A/MS Technology in Space Equipment
- Barriers to A/MS Integration for Space
- Facilitating Satellite Specific IC Development
- Realising Satellite Specific IC Development
- Conclusion

What is the space interest in semiconductor technology?

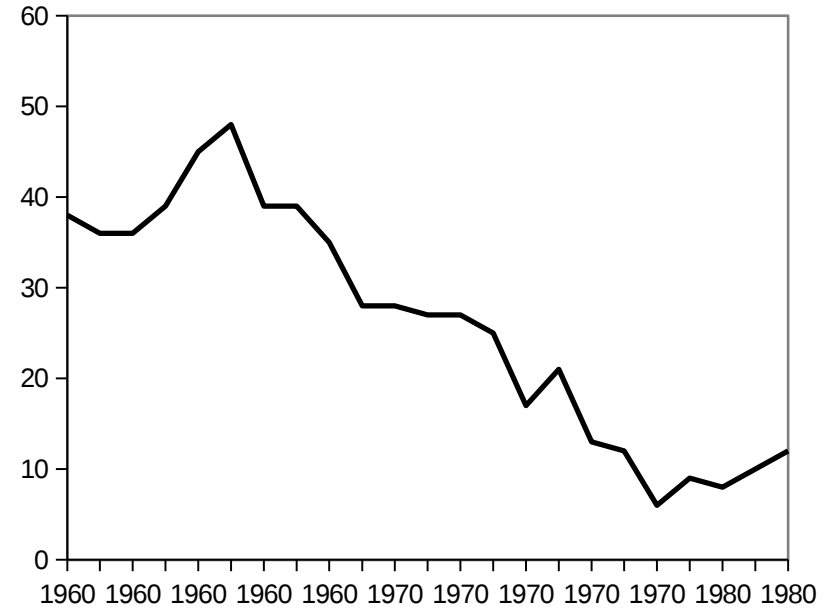
Miniaturisation

From the early 1960s a strong commitment to miniaturisation by the space, aerospace and military market is evident from the government share of semiconductor output [1].

2011 Semiconductor Market Figures

- €311 360 Million total
- € 31 000 Million Industrial
- € 23 000 Million automotive
- € 3 800 Million military/aerospace
- € 559 Million space
- € 80 Million space Europe

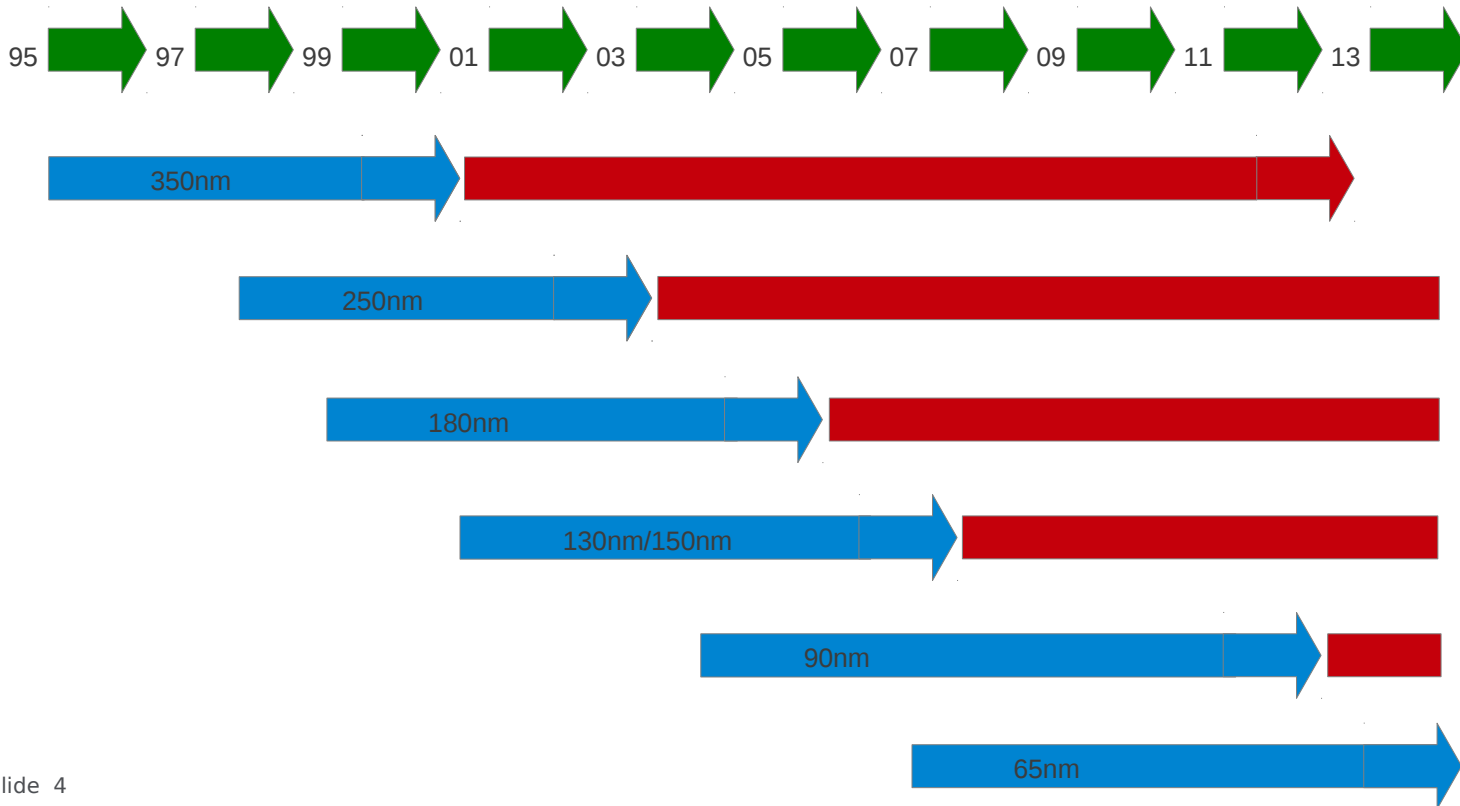
Government % of semiconductor output



How does the space semiconductor development compare to terrestrial ?

Space Semiconductor Technology Development

The average time lag for a space digital CMOS technology node is 7 years [2]



How does the analogue/mixed-signal (A/MS) semiconductor technology develop?

Mixed-Signal Technology Development

ADC performance over time [3] and per technology node [4]

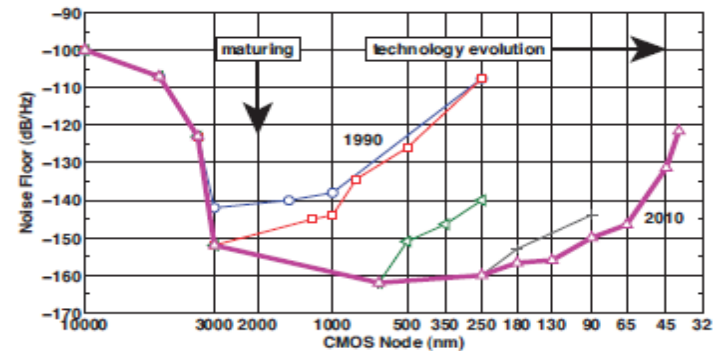
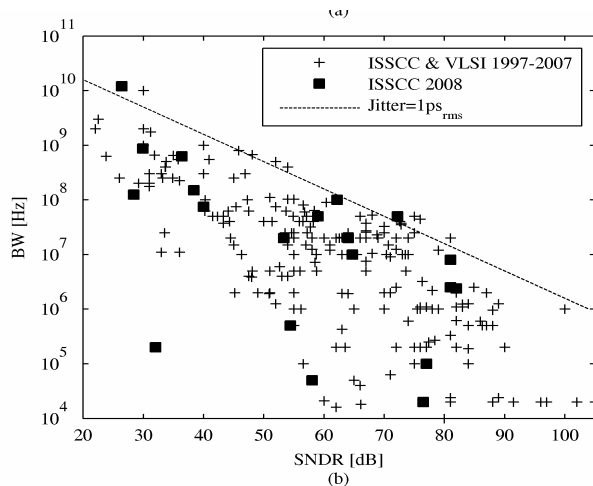


Figure 3. Relative noise floor vs. CMOS node. State-of-the-art envelopes at 1990 (○), 1995 (□), 2000 (◁), 2005 (+), and 2010 (△) illustrate the evolution of CMOS.

Convergence to CMOS semiconductor technology

After 2000 full ADC SNR is achieved in CMOS technology.

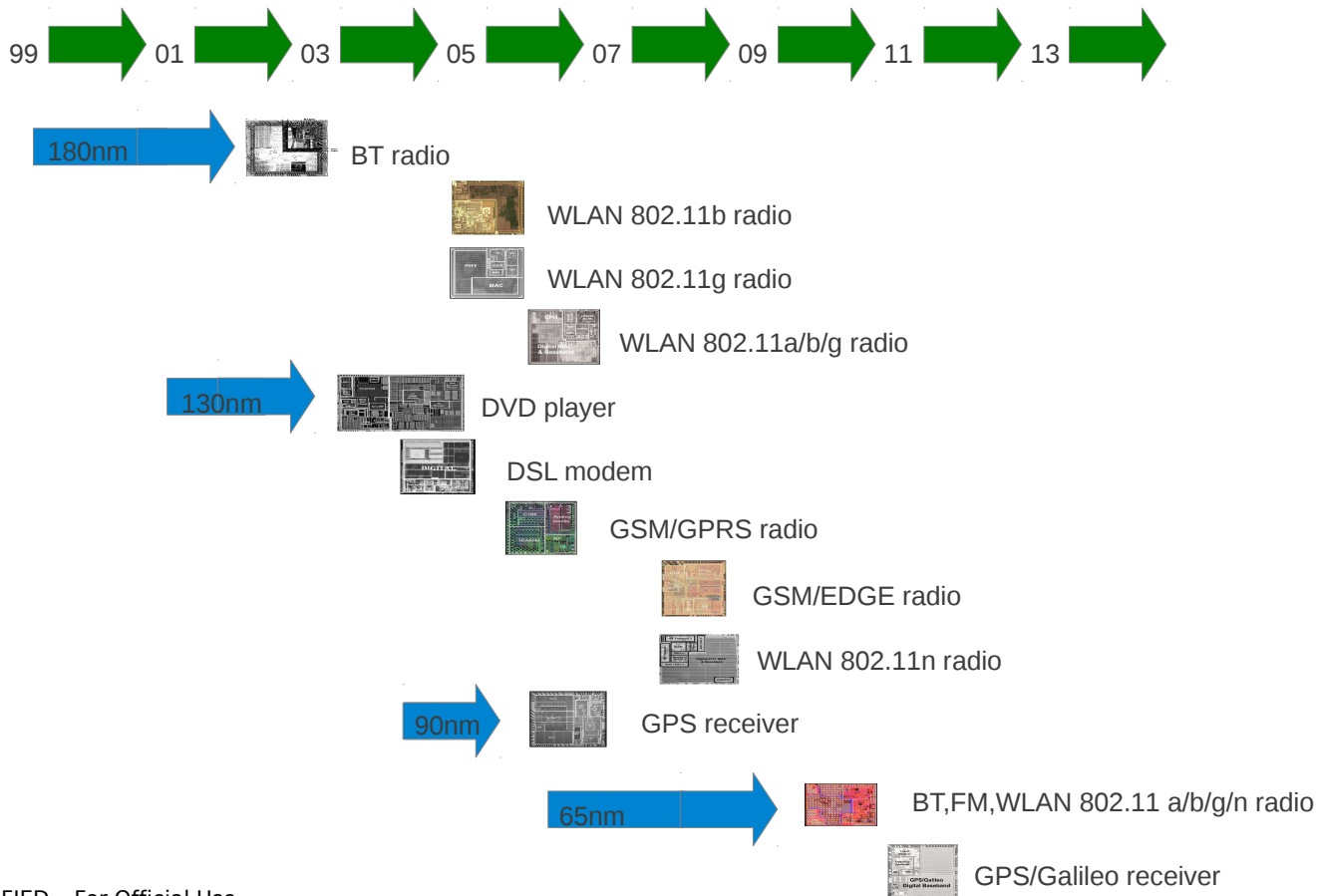
Mature mixed-signal technology is available.

Power consumption improves over time.

How does the analogue/mixed-signal (A/MS) semiconductor technology develop?

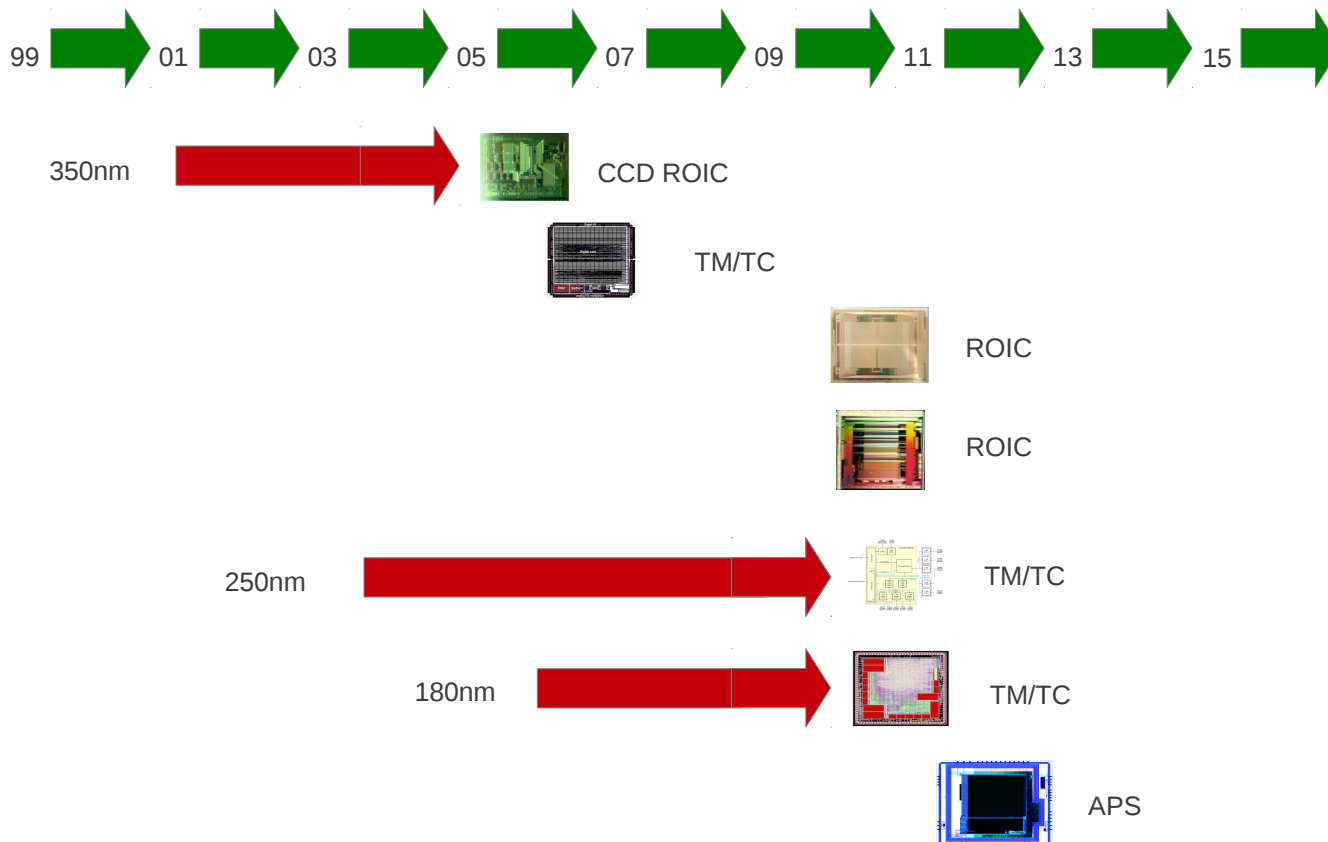
State of the art A/MS ASIC SoCs

First Mixed-Signal SoC 2 years after technology node ramp-up [5].



How does the space A/MS semiconductor technology develop?

Space A/MS ASIC SoCs Developed



[6]

How does the space A/MS semiconductor technology develop?

Space A/MS ASIC SoCs Development

1) The development time across technology nodes

SoC Type	Development time (yrs)
Terrestrial A/MS	2
Space Digital	6
Space A/MS	11

2) The performance of the A/MS blocks for space lags that of terrestrial.

A/MS semiconductor technology for space has not reached the state of the art

Number of diverse A/MS blocks

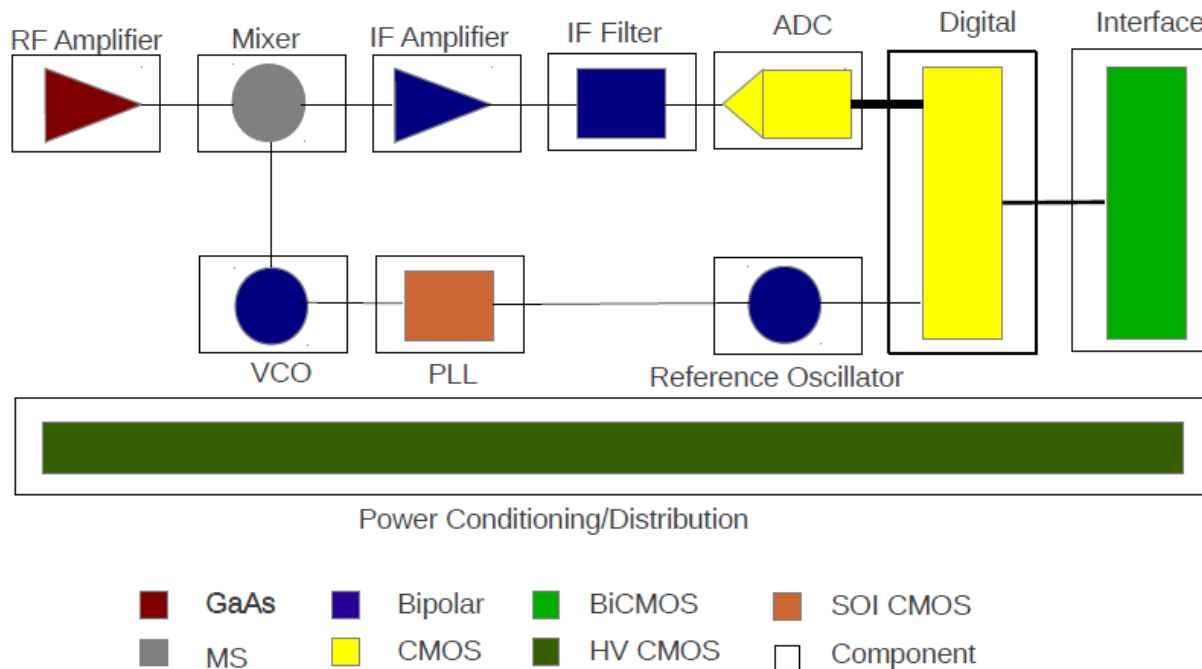
Number of connected A/MS blocks

Level of integration of A/MS functions is limited

3) The rate of A/MS technology development for space does not match that for terrestrial (consumer/industrial/automotive) use. This limits the growth of A/MS technology for space.

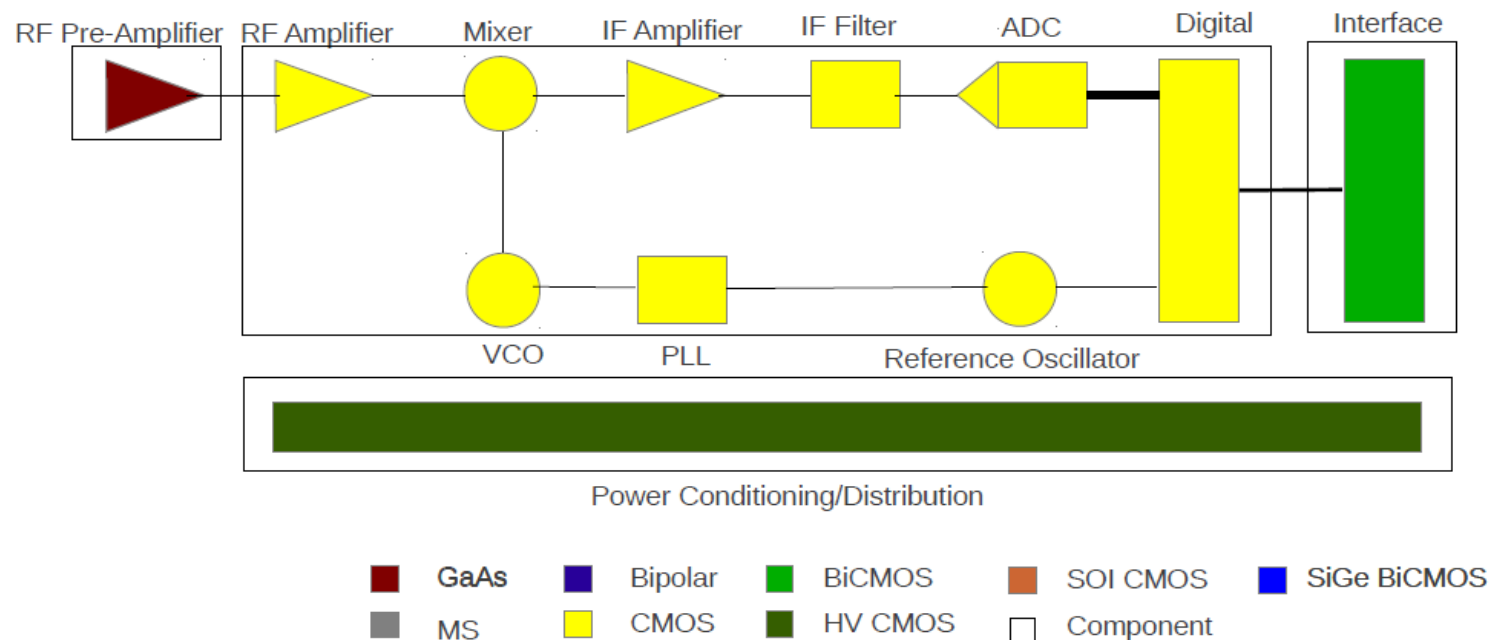
What is the current level of A/MS semiconductor integration in space?

L Band Receiver - Space (Discrete)



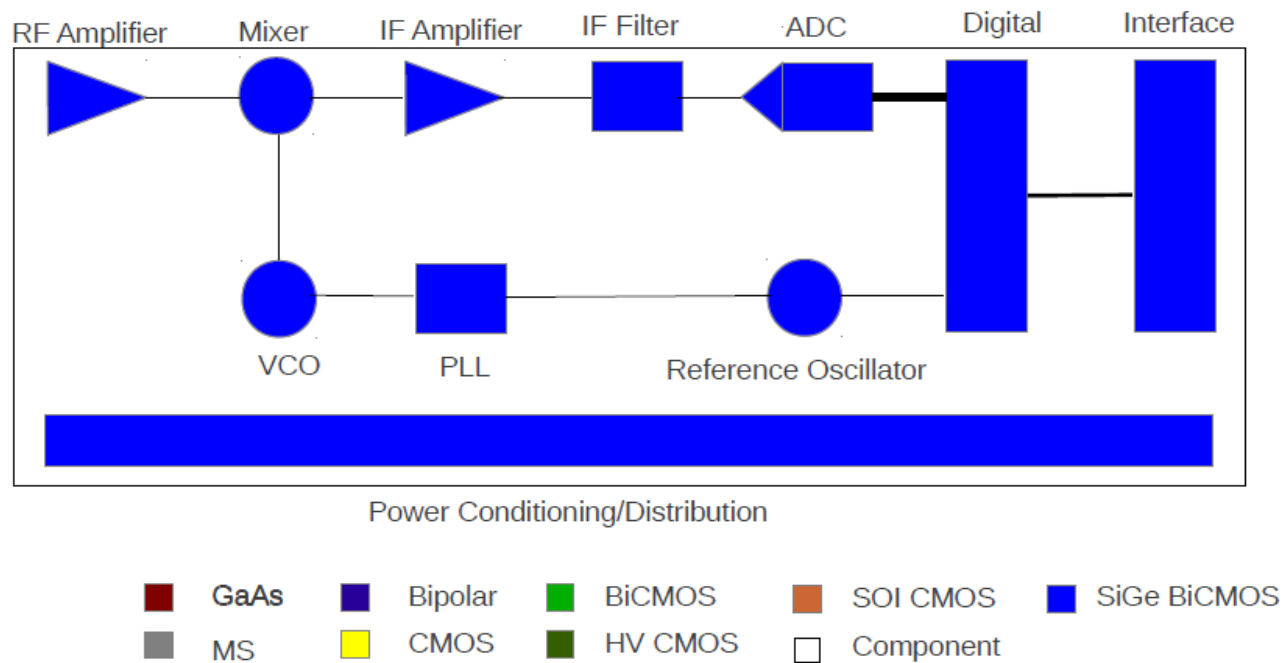
Can the same level of terrestrial A/MS semiconductor integration be attained for space?

L Band Receiver - Space (Integrated 1)



Can the same level of terrestrial A/MS semiconductor integration be attained for space?

L Band Receiver - Space (Integrated 2)



Can the same level of terrestrial A/MS semiconductor integration be attained for space?

L Band Receiver - Space (integrated)

Advantages

- Lower mass, smaller size
- Lower power
- Lower manufacture - assembly cost
- Higher reliability
- Higher functionality (lower cost per function)
- Higher performance (SNR, Bandwidth, Matching/Tracking)

Can the same level of terrestrial A/MS semiconductor integration be attained for space?

L Band Receiver - Space (integrated)

Disadvantages

- Higher development cost (component qualification)
- Higher development cost (unavailable qualified IP blocks - design iterations)
- Higher development risk (library/simulation limitations)
- Higher development risk (programmability/complexity)

For space the advantages of a discrete A/MS implementation with regard to risk and cost override those of an integrated implementation.

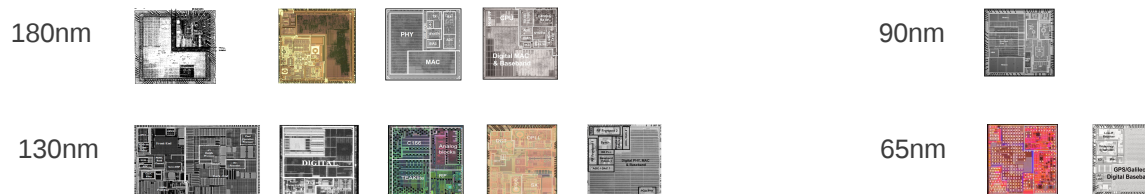
What allows terrestrial A/MS semiconductor integration?

Space and Terrestrial Semiconductor Application Differences

- Higher Environmental requirements (Radiation hardness, Temperature)
- Higher Reliability
- Specific Qualification Process
- Lower Area and Power requirements

- Lower production volume and lower ROI

For terrestrial applications the return of investment (ROI) makes the additional effort/complexity/risk and cost worthwhile to achieve an A/MS integrated implementation



What are the barriers to A/MS for space?

Cost

- Design of qualified IP blocks
- Design iterations
- Manufacture (low volume)
- Testing
- Qualification

Risk

- Limitations on the accuracy of library models
- Limitations of simulation tools
- Long design and manufacturing chain
 - no sub-block testing
 - late risk retirement

What are the cost elements preventing A/MS integration for space?

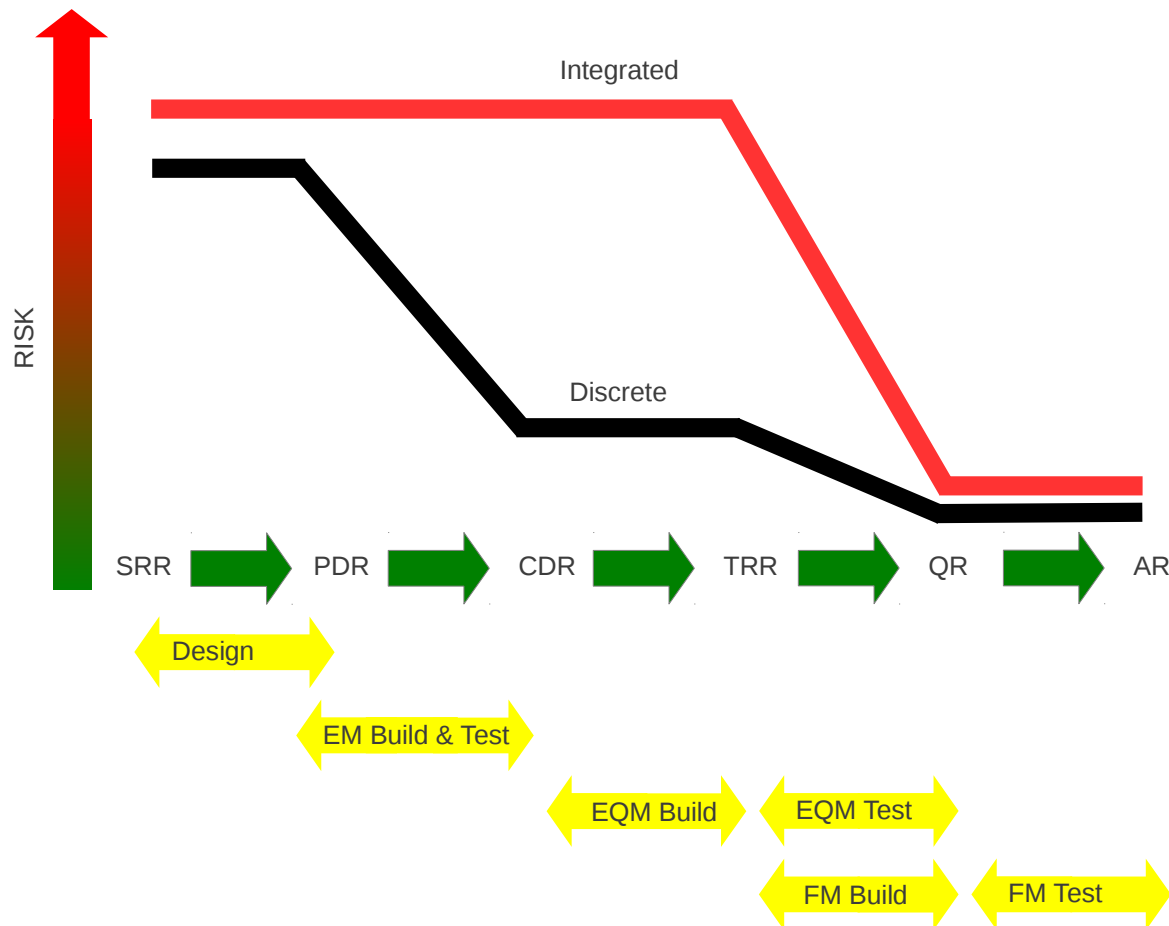
Development Cost

Fraction of Development Cost per Development Phase

50%	Design	
20%	Manufacture/Test/Screening	
	7.5%	Mask/Manufacture
	12.5%	Test/Screening
30%	Qualification	
	5%	Packaging
	5%	Burn in
	5%	Assembly Tests for Qualification
	5%	Reliability Tests for Qualification
	10%	Radiation Tests for Qualification

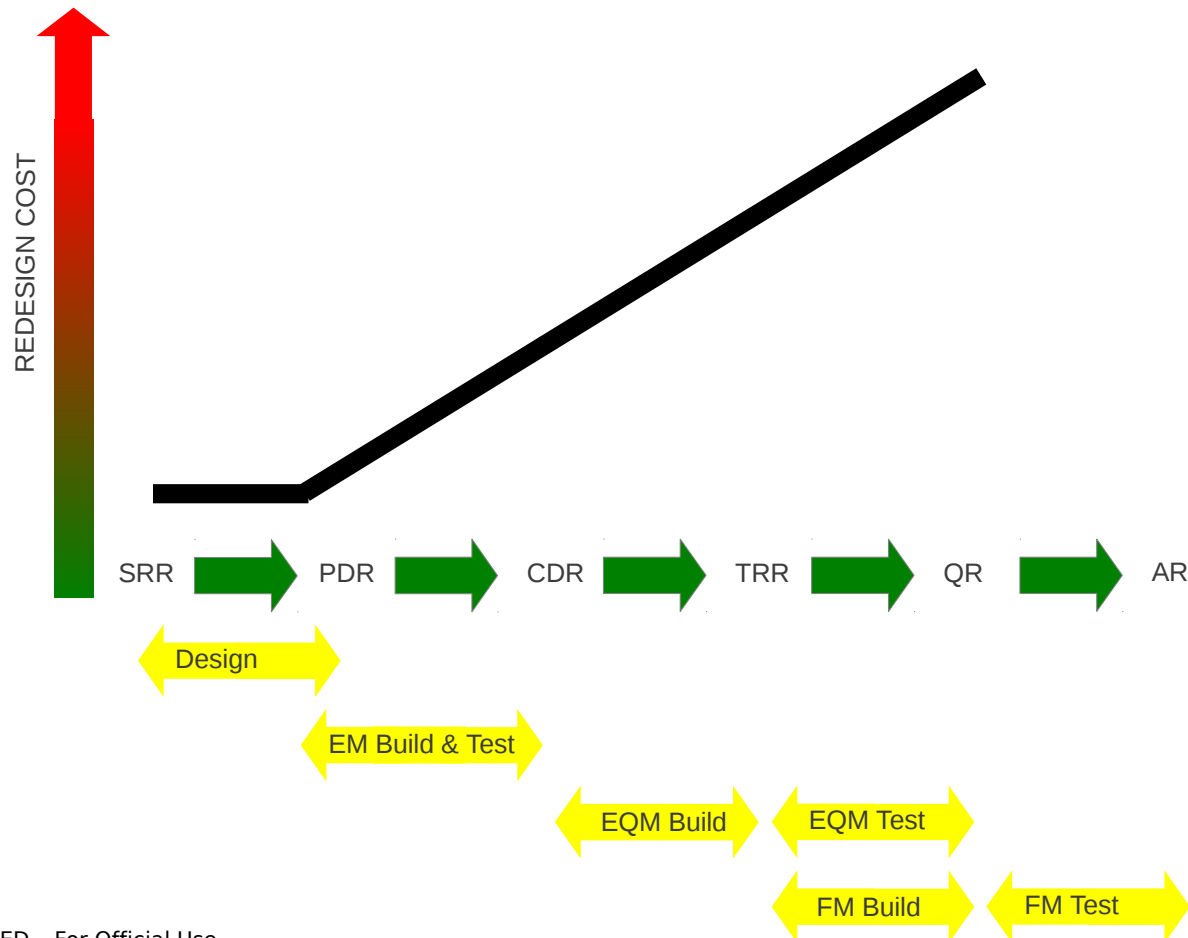
What barriers exist to the introduction of A/MS semiconductor technology for space?

Development Risk



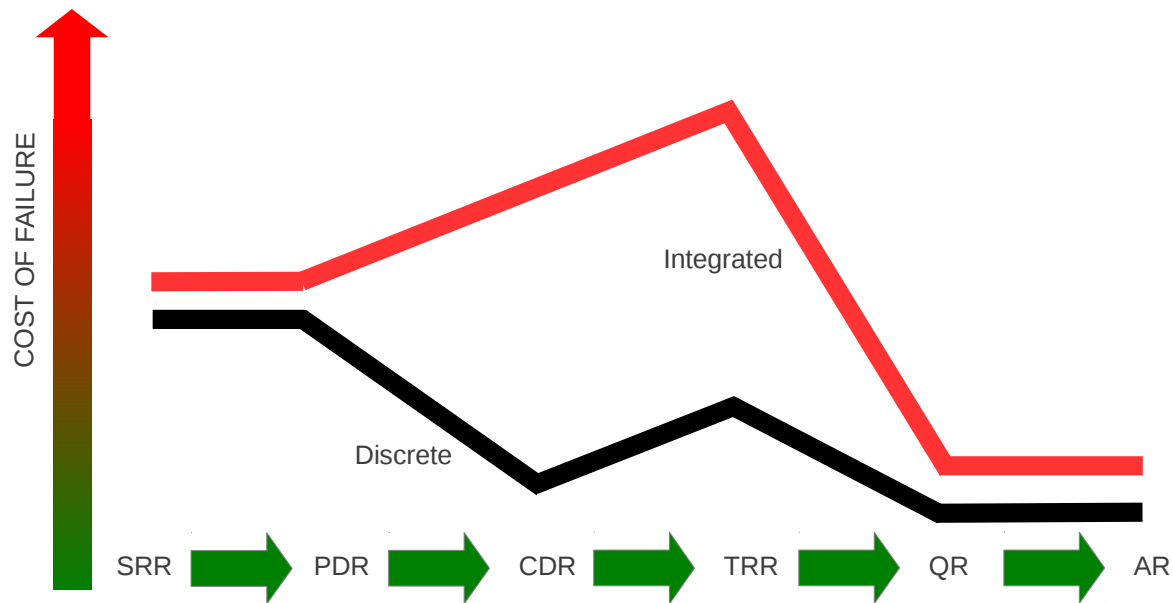
What barriers exist to the introduction of A/MS semiconductor technology for space?

Development Cost of Redesign



What barriers exist to the introduction of A/MS semiconductor technology for space?

Development Cost of Failure



The risk reduction for an ASIC development is not compatible to the expected risk reduction for a satellite development through engineering models. Only at the end of the qualification tests does the ASIC development risk reduce significantly

How can the advantages of the A/MS semiconductor technology be harnessed?

Increasing the Return On Investment

Classical approaches to increase ROI by making the component suitable for a larger number of applications

- Adaptability – adaptable hardware

- Configurability – FPGA

- Programmability – micro-controllers

- Platform development – system on chip

These approaches have been successfully applied in the digital domain.

In the space A/MS domain development is in progress for

- Adaptable ADC and DAC ASICs [7]

- Instrumentation platform – instrumentation and image processors ASICs [8]

- Programmable A/MS space micro-controllers [9]

How can the advantages of the A/MS semiconductor technology be harnessed?

Reducing Development Cost

- A/MS IP blocks are available / under development [8,10]

Reducing Manufacturing Cost

- Sharing wafers – MPW
- Sharing package tooling

Reducing Qualification Cost

- ESCC foundry capability approval []

Reducing Development Risk (library/simulation limitations)

- Improved libraries and tools are under development [11,12,13,14]

How can the advantages of the A/MS semiconductor technology be realised?

Reducing Development Risk

For the hypothetical case for the discrete L band receiver that

- 1) All the components are manufactured from one technology from one foundry
- 2) All the components have achieved qualification
- 3) The foundry has a capability approval for all the components
- 4) The components have well defined ports (50 Ohm or digital I/O)

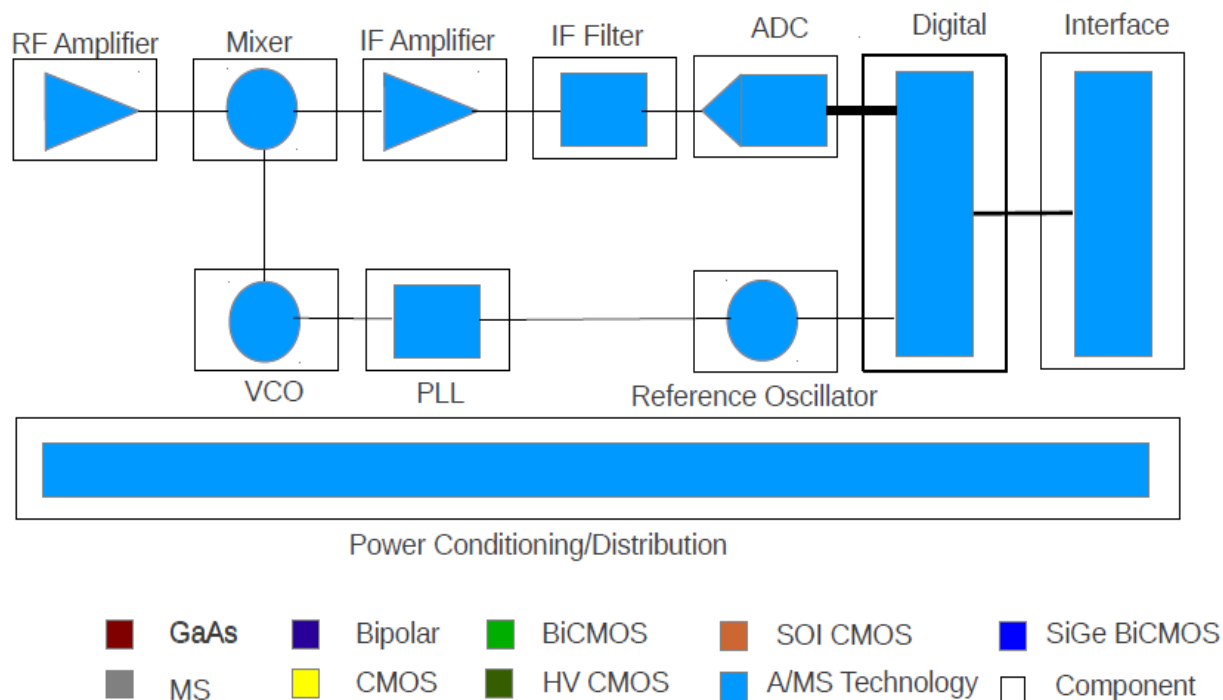
The EM of the L band receiver could be realised and proven to work with discrete components. These could also serve as EQM, PFM and FM parts.

However ...

Higher integration could also be achieved for the EQM by integrating the different components onto an ASIC.

How can the advantages of the A/MS semiconductor technology be realised?

L Band Receiver - Space



How can the advantages of the A/MS semiconductor technology be realised?

Reducing Development Risk

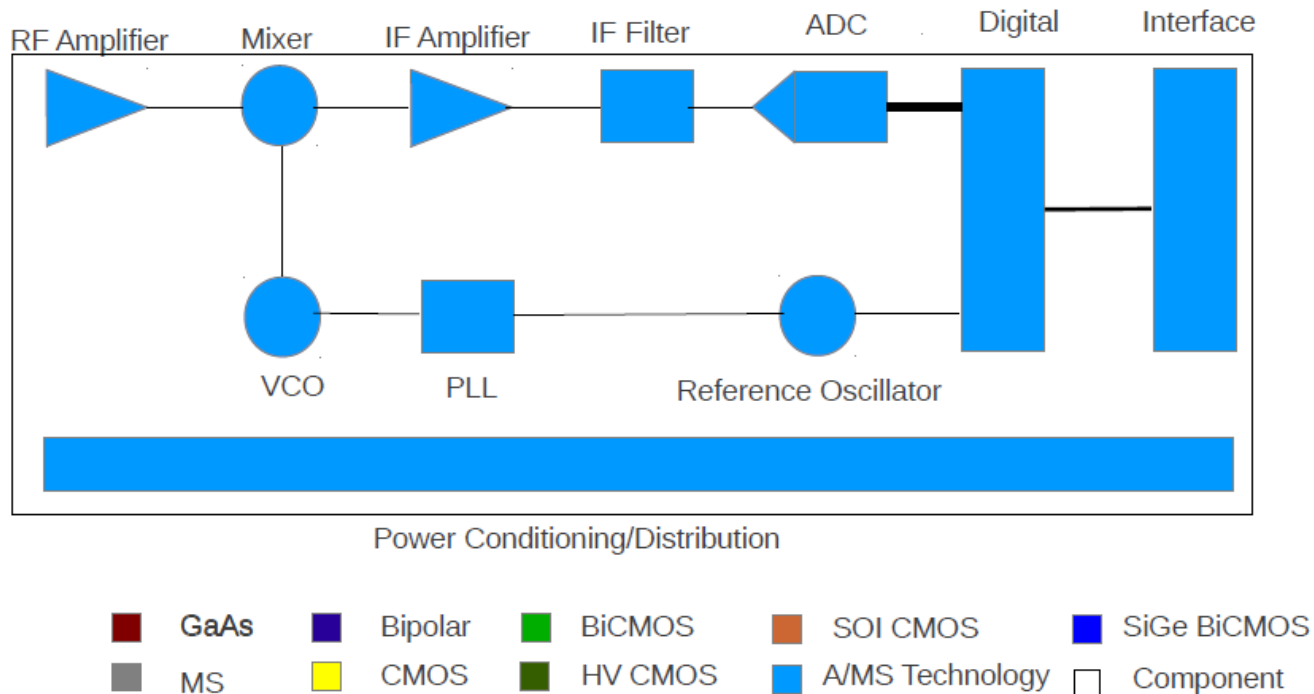
This integrated ASIC could be developed with a minimal risk

- 1) All the components/blocks have already achieved qualification with regard to functionality, performance, radiation hardness, reliability
- 2) The capability approval ensures that the repeated manufacture produces components/blocks of identical quality.
- 3) Well defined port impedances of the components/blocks ensures that the interfaces are well controlled
- 4) The EM has demonstrated the connected blocks interface, function and perform

This approach would be compatible with the satellite development programme, which ensures that at each milestone the development risk is reduced.

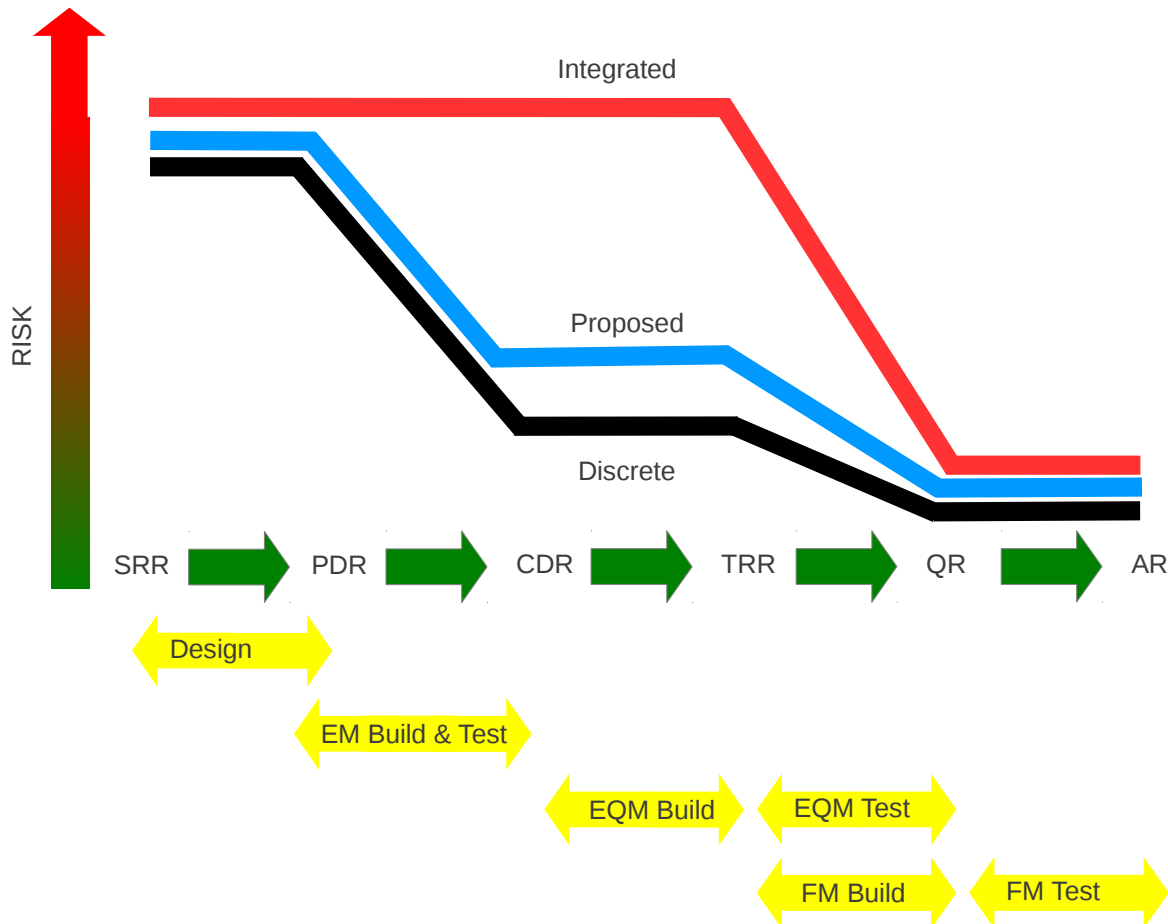
How can the advantages of the A/MS semiconductor technology be realised?

L Band Receiver - Space



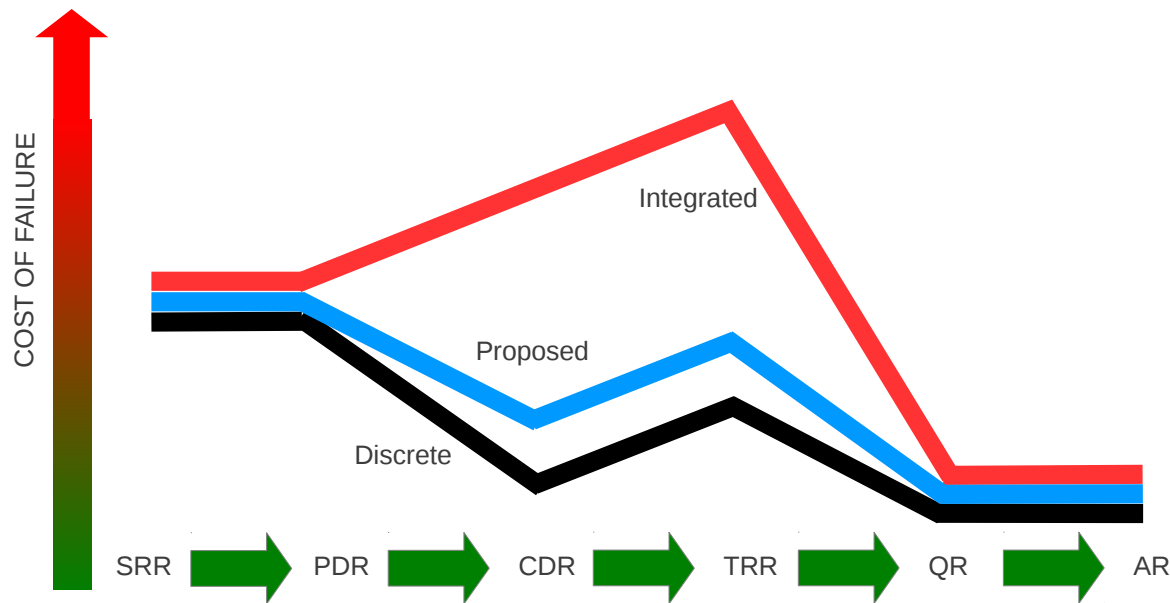
How can the advantages of the A/MS semiconductor technology be realised?

Development Risk



How can the advantages of the A/MS semiconductor technology be realised?

Development Cost of Failure



The proposed ASIC development systematically reduces the risk at CDR through EM. The EM is the basis for the integrated EQM and FM. The potential cost of failure can be significantly reduced.

How can the advantages of the A/MS semiconductor technology be realised?

Increasing integration/enabling miniaturisation

A comprehensive A/MS block library available from one/several companies

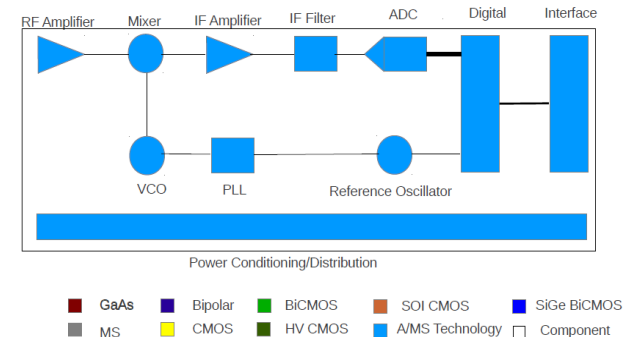
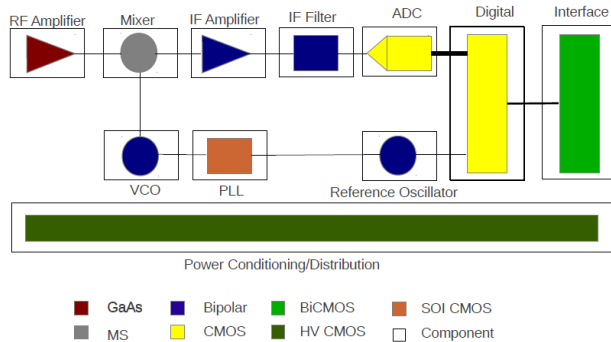
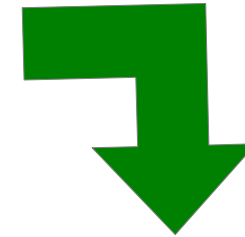
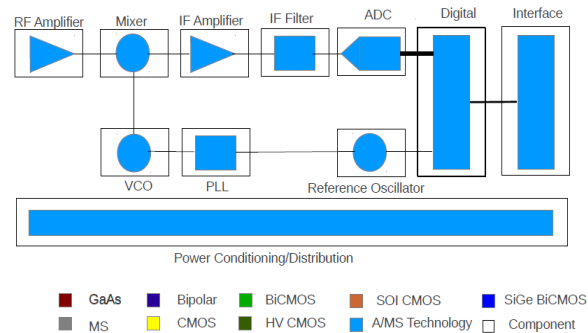
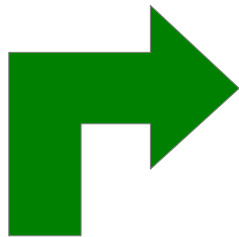
- The blocks ports should be defined and demonstrated to operate with other blocks on/off chip
- The blocks should provide provide a maximum of configurability/adaptability to limit their number
- The blocks should be ESCC space qualified for functionality / performance / radiation hardness / reliability for each operating mode

A verification/integration flow should be available on the technology

A ESCC capability approved foundry

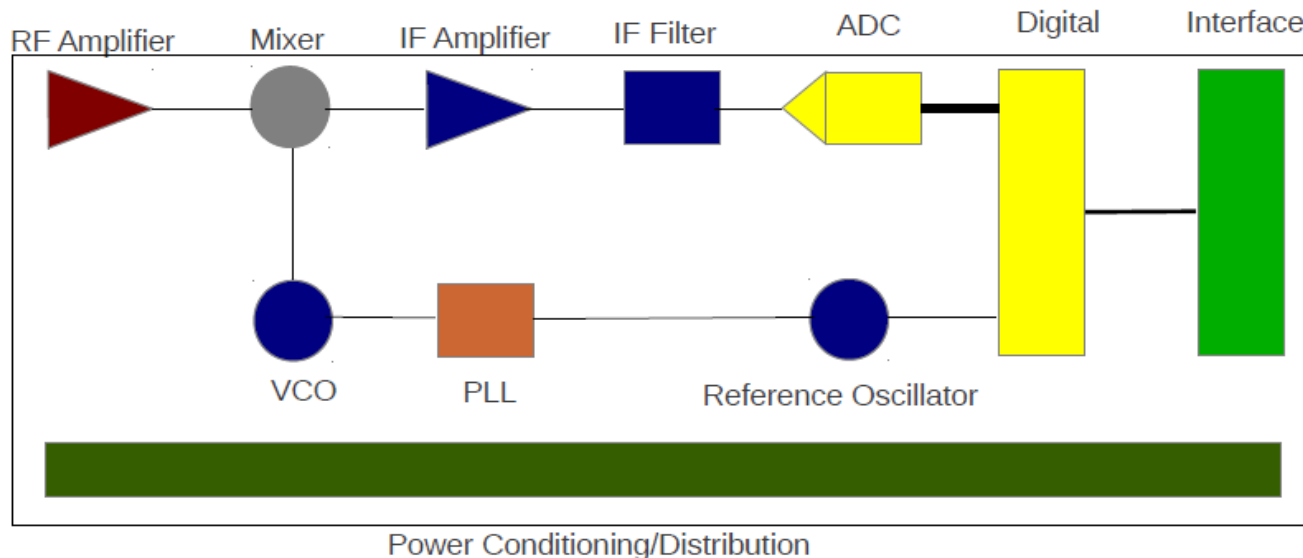
How can the advantages of the A/MS semiconductor technology be realised?

Increasing integration/enabling miniaturisation



How can the advantages of the A/MS semiconductor technology be realised?

Increasing integration/enabling miniaturisation



- | | | | |
|------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|
|  Provider 1 |  Provider 3 |  Provider 5 |  Provider 7 |
|  Provider 2 |  Provider 4 |  Provider 6 |  Component |

Indicated that a technology gap exists in the adoption of A/MS technology for space

Indicated that this technology gap is related to the development risk inherent to A/MS ASIC development that is incompatible to satellite development programmes.

Proposed a Satellite Specific IC development flow that meets satellite development requirement with regard to risk containment.

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